

## SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, AND SEMICONDUCTOR MOUNTING STRUCTURE

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### Abstract

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**PROBLEM TO BE SOLVED:** To prevent a signal delay due to a wiring length and improve a heat radiation efficiency, in a semiconductor device or semiconductor module which is constructed into a three-dimensional structure by folding up a flexible wiring board.

**SOLUTION:** The semiconductor device or semiconductor module comprises the flexible wiring board which has bending sections and has a first principal plane (front principal plane) that can be mounted with a plurality of semiconductor chips at prescribed intervals; and at least one set of laminates composed of stacked semiconductor chips adjacent each other and mounted on the first principal plane (front principal plane) of the flexible wiring board, which is formed as a result of folding up the flexible wiring board at the bending sections, with wirings of the same function of the laminates being electrically connected by short cut wiring boards.

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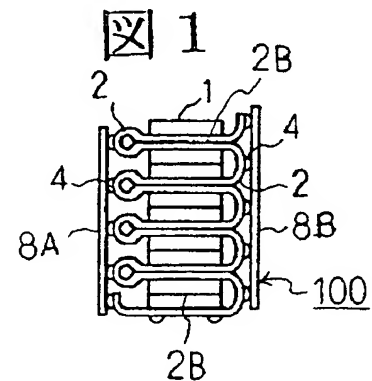
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(54) 【発明の名称】 半導体装置及びその製造方法並びに半導体実装方法

(57) 【要約】

【課題】 可撓性配線基板を折り畳んで立体構造（三次元）にした半導体装置もしくは半導体モジュールにおいて、配線長による信号遅延を防止する。放熱効率を向上する。

【解決手段】 折り曲げ部を有し、複数の半導体チップが第1主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲部で折り曲げられて前記可撓性配線基板の第1主面（表主面）に搭載された隣合せの半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線をショートカット配線基板で電気的に接続した半導体装置もしくは半導体モジュールである。



## 【特許請求の範囲】

【請求項1】 折り曲げ部を有し、複数の半導体チップが第1主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面に搭載された隣合せの半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線を電気的に接続するショートカット配線基板とを備えたことを特徴する半導体装置。

【請求項2】 折り曲げ部を有し、複数の半導体チップが第1主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面に搭載された隣合せの半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線を電気的に接続するショートカット配線基板と、前記可撓性配線基板の第2主面に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板の配線ランドとを電気的に接続する手段とを備えたことを特徴する半導体装置。

【請求項3】 折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第1主面に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカット配線基板で電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項4】 折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第1主面に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第2主面に設けられた前記積層体の同一機能の配線の共通端子とを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続する工程と、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカット配線基板で電気的に接続する工程と、前記共通端子と実装基板の配線ランドとを電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項5】 折り曲げ部を有し、複数の半導体チップが第1主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面に搭載された隣合せの半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部とを備えたことを特徴する半導体装置。

【請求項6】 折り曲げ部を有し、複数の半導体チップが第1主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面に搭載された隣合せの半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部と、前記可撓性配線基板の第2主面に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板の配線ランドとを電気的に接続する手段とを備えたことを特徴する半導体装置。

【請求項7】 折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第1主面に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項8】 折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第1主面に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第2主面に設けられた前記積層体の同一機能の配線の共通端子とを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板の配線ランドとを電気的に接続す

る工程とを備えたことを特徴する半導体装置の製造方法。

【請求項9】 四つ折り曲げ部を有し、複数の半導体チップが第1主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面に搭載された半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部とを備えたことを特徴する半導体装置。

【請求項10】 四つ折り曲げ部を有し、複数の半導体チップが第1主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面に搭載された半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部と、前記可撓性配線基板の第2主面に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板のランドとを電気的に接続する手段とを備えたことを特徴する半導体装置。

【請求項11】 四つ折り曲げ部を有し、該四つ折り曲げ部で折り曲げられると、その第1主面に搭載される半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記四つ折り曲げ部で折り曲げて前記可撓性配線基板の第1主面に搭載された半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項12】 四つ折り曲げ部を有し、四つ折り曲げ部で折り曲げられると、その第1主面に搭載される隣合の半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第2主面に形成された前記積層体の同一機能の配線の共通端子を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続する工程と、前記電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面に搭載された隣合の半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線同志を電気的に接続する工程と、前記積層体

の同一機能の配線の共通端子と実装基板のランドとを電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項13】 四つ折り曲げ部または折り曲げ部を有し、複数の半導体チップが第1主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面に搭載された半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した半導体装置であって、前記半導体チップが重ね合わされた積層体間に冷却路を設けたことを特徴とする半導体装置。

【請求項14】 四つ折り曲げ部または折り曲げ部を有し、複数の半導体チップが第1主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面に搭載された半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線ランド同志を電気的に接続し、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続した半導体装置であって、前記半導体チップが重ね合わされた積層体間に冷却路を設け、前記可撓性配線基板の第2主面に前記積層体の同一機能の配線の共通端子を設け、該共通端子と実装基板の配線ランドとを電気的に接続したことを特徴とする半導体装置。

【請求項15】 四つ折り曲げ部または折り曲げ部を有し、該四つ折り曲げ部または折り曲げ部で折り曲げられると、その第1主面に搭載される半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げて前記可撓性配線基板の第1主面に搭載された半導体チップを重ね合わされて積層する工程と、前記半導体チップが重ね合わされた積層体間に熱伝導性接着テープと熱吸収パッドで冷却路を形成する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項16】 四つ折り曲げ部または折り曲げ部を有し、四つ折り曲げ部で折り曲げられると、その第1主面に搭載される隣合の半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の

第2主面に設けられた前記積層体の同一機能の配線の共通端子を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記半導体チップが重ね合わされた積層体間に熱伝導性接着テープと熱吸収パッドで冷却路を形成する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、面実装型半導体装置もしくは半導体モジュール及びその製造方法に関し、特に、可撓性配線基板（フレキシブル配線基板）またはリードフレーム上に複数の半導体チップを搭載し、隣り合わせた半導体チップもしくは前記搭載された半導体チップを背中合わせにして重ね合せ、積層する技術に適用して有効な技術に関するものである。

【0002】

【従来の技術】従来の小型化・高集積化を図る構造の半導体装置として、例えば、特開平9-181215号公報に記載されるように、可撓性配線基板（フレキシブル配線基板）の重量部に半導体チップを組み込んだ封止体を有するとともに、可撓性配線基板の半導体チップ実装用外部端子（半導体チップ実装用ランド）が設けられた面の反対側面にも半導体チップを組み込んだパッケージ（封止体）を配置したものが提案されている（図22～24参照）。

【0003】

【発明が解決しようとする課題】本発明者は、前記の従来技術を検討した結果、以下の問題点を見いだした。前記従来技術では、構造的には立体構造（三次元）で実装面積の小型化や高集積化が可能であるが、基板的には平面状（二次元）の基板を折り畳んだだけで配線長は、通常の平面基板と変わらないため、配線長による信号遅延の問題があった。また、狭い空間に多数の半導体チップ（ICチップ）等を積層したパッケージのため内部の熱が逃げにくく、動作不良等の問題があった。また、BGA（Ball Grid Array）の半田ボール端子はリード端子と違い変形できないため、実装基板の変形や膨張によってクラック破断を起すという問題があった。

【0004】本発明の目的は、基板を折り畳んで立体構造（三次元）にした半導体装置もしくは半導体モジュールにおいて、配線長による信号遅延を防止することが可

能な技術を提供することにある。本発明の他の目的は、基板を折り畳んで立体構造（三次元）にした半導体装置もしくは半導体モジュールにおいて、放熱効率を向上することが可能な技術を提供することにある。本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述及び添付図面によって明らかになるであろう。

【0005】

【課題を解決するための手段】本願において開示される発明の概要を簡単に説明すれば、以下のとおりである。第1の発明は、折り曲げ部を有し、複数の半導体チップが第1主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面（表主面）に搭載された隣合せの半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線を電気的に接続するショートカット配線基板とを備えた半導体装置である。

【0006】第2の発明は、折り曲げ部を有し、複数の半導体チップが第1主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面（表主面）に搭載された隣合せの半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線を電気的に接続するショートカット配線基板と、前記可撓性配線基板の第2主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板の配線ランドとを電気的に接続する手段とを備えた半導体装置である。

【0007】第3の発明は、折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第1主面（表主面）に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面（表主面）に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカット配線基板で電気的に接続する工程とを備えた半導体装置の製造方法である。

【0008】第4の発明は、折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第1主面（表主面）に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第2主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子とを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体

チップの外部電極（パッド）とを電気的に接続する工程と、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面（表主面）に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカット配線基板で電気的に接続する工程と、前記共通端子と実装基板の配線ランドとを電気的に接続する工程とを備えた半導体装置の製造方法である。

【0009】第5の発明は、折り曲げ部を有し、複数の半導体チップが第1主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面（表主面）に搭載された隣合せの半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部とを備えた半導体装置である。

【0010】第6の発明は、折り曲げ部を有し、複数の半導体チップが第1主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面（表主面）に搭載された隣合せの半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部と、前記可撓性配線基板の第2主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板の配線ランドとを電気的に接続する手段とを備えた半導体装置である。

【0011】第7の発明は、折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第1主面（表主面）に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面（表主面）に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えた半導体装置の製造方法である。

【0012】第8の発明は、折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第1主面（表主面）に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第

2主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子とを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面（表主面）に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板の配線ランドとを電気的に接続する工程とを備えた半導体装置の製造方法である。

【0013】第9の発明は、四つ折り曲げ部を有し、複数の半導体チップが第1主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面（表主面）に搭載された半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部とを備えた半導体装置である。

【0014】第10の発明は、四つ折り曲げ部を有し、複数の半導体チップが第1主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面（表主面）に搭載された半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部と、前記可撓性配線基板の第2主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板のランドとを電気的に接続する手段とを備えた半導体装置である。

【0015】第11の発明は、四つ折り曲げ部を有し、該四つ折り曲げ部で折り曲げられると、その第1主面（表主面）に搭載される半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記四つ折り曲げ部で折り曲げて前記可撓性配線基板の第1主面（表主面）に搭載された半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えた半導体装置の製造方法である。

【0016】第12の発明は、四つ折り曲げ部を有し、四つ折り曲げ部で折り曲げられると、その第1主面（表



主面)に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第2主面(裏主面)に形成された前記積層体の同一機能の配線の共通端子を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極(パッド)とを電気的に接続する工程と、前記電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面(表主面)に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続する工程とを備えた半導体装置の製造方法である。

【0017】第13の発明は、四つ折り曲げ部または折り曲げ部を有し、複数の半導体チップが第1主面(表主面)に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面(表主面)に搭載された半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した半導体装置であって、前記半導体チップが重ね合わされた積層体間に冷却路を設けた半導体装置である。

【0018】第14の発明は、四つ折り曲げ部または折り曲げ部を有し、複数の半導体チップが第1主面(表主面)に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げられて前記可撓性配線基板の第1主面(表主面)に搭載された半導体チップが重ね合わされた少なくとも1組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続し、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続した半導体装置であって、前記半導体チップが重ね合わされた積層体間に冷却路を設け、前記可撓性配線基板の第2主面(裏主面)に前記積層体の同一機能の配線の共通端子を設け、該共通端子と実装基板の配線ランドとを電気的に接続した半導体装置である。

【0019】第15の発明は、四つ折り曲げ部または折り曲げ部を有し、該四つ折り曲げ部または折り曲げ部で折り曲げられると、その第1主面(表主面)に搭載される半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線同志を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極(パッド)とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配

線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げて前記可撓性配線基板の第1主面(表主面)に搭載された半導体チップを重ね合わされて積層する工程と、前記半導体チップが重ね合わされた積層体間に熱伝導性接着テープと熱吸収パッドで冷却路を形成する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えた半導体装置の製造方法である。

【0020】第16の発明は、四つ折り曲げ部または折り曲げ部を有し、四つ折り曲げ部で折り曲げられると、その第1主面(表主面)に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも1組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第2主面(裏主面)に設けられた前記積層体の同一機能の配線の共通端子を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極(パッド)とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第1主面(表主面)に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記半導体チップが重ね合わされた積層体間に熱伝導性接着テープと熱吸収パッドで冷却路を形成する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続する工程とを備えた半導体装置の製造方法である。

#### 【0021】

【発明の実施の形態】以下、本発明について、図面を参照して実施の形態(実施例)とともに詳細に説明する。なお、実施例を説明するための全図において、同一機能を有するものは同一符号を付け、その繰り返しの説明は省略する。

【0022】(実施例1)図1は本発明の実施例1の半導体装置の概要構成を示す正面図であり、図2は本実施例1の半導体装置を実装基板に実装した正面図である。本実施例1の半導体装置は、図1に示すように、折り曲げ部を有する可撓性配線基板2の表主面(第1主面)に所定の間隔で複数の半導体チップ(1Cチップ)1が搭載され、前記可撓性配線基板2の前記折り曲げ部で折り曲げられて、前記可撓性配線基板2の表主面に搭載された隣合せの半導体チップ1が背中合わせに重ね合わされ、接着材(又は接着テープ)2Bで固定される。さらに、前記可撓性配線基板2の前記折り曲げ部2Aで折り曲げられて、次の1組の積層体が積層される。このようにして複数組の積層体が構成される。該複数組の積層体の前記各種層体の同一機能の配線をショートカット配線

基板8で電氣的に接続して前記可撓性配線基板2の配線長をショートカットする。前記可撓性配線基板2の厚さは、例えば、 $75\mu\text{m}$ 、Cu配線の厚さは $35\mu\text{m}$ である。

【0023】図2に示すように、本実施例1の半導体装置100は、前記可撓性配線基板2の裏主面(第2主面)に設けられている実装用半田ボール端子(配線の共通端子)7と実装基板9の半導体装置実装用ランド9Aとを電氣的に接続して前記実装基板9に実装される。

【0024】次に、本実施例1の半導体装置の製造方法について説明する。図3は前記可撓性配線基板2の配線構成を示す表平面図、図4は前記可撓性配線基板2の配線構成を示す裏平面図、図5は前記可撓性配線基板2上に半導体チップ1を搭載した状態を示す全体平面図、図6は図5の側面図、図7は1個の半導体チップ1を前記可撓性配線基板2上に搭載した状態を示す断面図、図8は前記ショートカット配線基板8A、8Bの一方の配線基板8Aと他方の配線基板8Bの配線構成を示す平面図、図9は前記ショートカット配線基板8A、8Bの一方の配線基板8Aを前記可撓性配線基板2の配線に接続した状態を示す図である。

【0025】図3～図9において、1は半導体チップ(ICチップ)、1Aは半導体チップの外部電極(パッド上のAuパンプ)、2は可撓性配線基板(フレキシブル配線基板)、2Aは折り曲げ部、3は配線、4はショートカット配線接続用Auパンプ、5はビア、6は半導体チップ搭載用ランド、7は実装用半田ボール端子(共通配線外部端子)、8A、8Bはショートカット配線基板、8A1、8B1はショートカット配線ランド、9は実装基板、9Aは実装基板上の半導体装置実装用ランド、10は封止材、11はフレキシブル基板テープ、12は絶縁膜(保護膜)である。

【0026】まず、図3に示すような可撓性配線基板(フレキシブル配線基板)2を製造する。前記可撓性配線基板(フレキシブル配線基板)2の製造は、図3に示すように、フレキシブル基板テープ11に配線を形成し、その上に絶縁膜(保護膜)12を被覆する。この配線が形成されたフレキシブル基板テープ11の表主面に、半導体チップ1の同一機能の半導体チップ搭載用ランド6を接続する配線3、半導体チップ1の同一機能の半導体チップ搭載用ランド6を接続するショートカット配線接続用Auパンプ4、前記配線3を通すビア5、及び半導体チップ搭載用ランド6をそれぞれ所定位置に形成する。前記フレキシブル基板テープ11の裏主面には、図4に示すように、半導体チップ1の同一機能の半導体チップ搭載用ランド6を接続する配線3及びショートカット配線接続用Auパンプ4並びに実装用半田ボール端子(共通配線外部端子)7を形成する。

【0027】本実施例1の半導体装置の製造方法は、前記図3に示すような可撓性配線基板(フレキシブル配線

基板)2を用意する。次に、図5及び図6に示すように、前記可撓性配線基板2の表主面に所定の間隔で形成された半導体チップ搭載用ランド6上に、半導体チップの外部電極(パッド上のAuパンプ)1Aを電氣的に接続して複数の半導体チップ(ICチップ)1を搭載する。すなわち、半導体チップ(ICチップ)1は、図7に示すように、半導体チップ搭載用ランド6と外部電極(パッド上のAuパンプ)1Aとを電氣的に接続し、その接続部を封止材(封止樹脂)10で封止する。

【0028】前記複数の半導体チップ1が搭載された前記可撓性配線基板2の前記折り曲げ部2Aで、図6に示す矢印方向に折り曲げられて、前記可撓性配線基板2の表主面に搭載された隣合せの半導体チップ1が背中合わせに重ね合せ、接着材(又は接着テープ)2Bで固定する。さらに、前記可撓性配線基板2の前記折り曲げ部2Aで折り曲げて、ショートカット配線接続用Auパンプ4とショートカット配線接続用ランド4Aとを接続し、次の1組の積層体を積層する。このようにして複数組の積層体を構成する。

【0029】前記複数組の積層体の前記各積層体の同一機能の配線を、図9に示すように、まず、図8(a)に示すショートカット配線基板8Aで左側の積層体の同一機能の配線のショートカット配線接続用Auパンプ4を電氣的に接続し、次に、図8(b)に示すショートカット配線基板8Bのショートカット配線ランド8B1と右側の積層体の同一機能の配線のショートカット配線接続用Auパンプ4を電氣的に接続する。これにより前記可撓性配線基板2の配線長をショートカットすることができる。このようにして、図1に示すような半導体装置100を完成する。前記半導体装置100は、図2に示すように、前記積層体の同一機能の配線の共通端子である実装用半田ボール端子(配線の共通端子)7と実装基板9上の半導体装置実装用ランド9Aとを電氣的に接続する。

【0030】以上説明したように本実施例1によれば、折り曲げ可能な可撓性配線基板2を用い、前記各積層体の同一機能の配線をショートカット配線基板8A、8Bで電氣的に接続して、前記可撓性配線基板2の配線長をショートカットするので、配線長による信号遅延を防止することができる。また、配線基板を折り畳んで立体構造(三次元)にした半導体装置において、前記各積層体の同一機能の配線をショートカット配線基板8A、8Bにより積層体内部の熱の放熱効率を向上させることができる。また、実装用半田ボール端子部以外の基板の両面にICチップを両面実装することも可能である。

【0031】(実施例2)図10は本発明の実施例2の半導体装置の概要構成を示す正面図であり、図11は本実施例2の半導体装置を実装基板に実装した正面図である。本実施例2の半導体装置は、前記実施例1のショートカット配線基板8A、8Bを省略した実施例である。



すなわち、図10に示すように、折り曲げ部2Aを有する可撓性配線基板2の表主面に所定の間隔で複数の半導体チップ（ICチップ）1が搭載され、前記可撓性配線基板2の前記折り曲げ部2Aで折り曲げられて、前記可撓性配線基板2の表主面（第1主面）に搭載された隣合の半導体チップ2が背中合わせに重ね合わせられ、接着材（又は接着テープ）2Bで固定される。さらに、前記可撓性配線基板2の前記折り曲げ部2Aで折り曲げられて、ショートカット配線接続用Auパンプ4とショートカット配線接続用ランド4Aとを接続し、次の1組の積層体が積層される。このようにして複数組の積層体が構成される。該複数組の積層体の前記各積層体の同一機能の配線のショートカット配線接続用ランド4Aとショートカット配線接続用Auパンプ4とを電気的に接続して前記可撓性配線基板2の配線長をショートカットする。

【0032】図11に示すように、本実施例2の半導体装置200は、前記可撓性配線基板2の裏主面（第2主面）に設けられている実装用半田ボール端子（配線の共通端子）7と実装基板9の半導体装置実装用ランド9Aとを電気的に接続して前記実装基板9に実装される。

【0033】次に、本実施例2の半導体装置の製造方法について説明する。図12は前記可撓性配線基板2の配線構成を示す表平面図、図13は前記可撓性配線基板2の配線構成を示す裏平面図、図14は前記可撓性配線基板2上に半導体チップ1を搭載した状態を示す全体平面図、図15は図14の側面図、図16は1個の半導体チップ1を前記可撓性配線基板2の表主面に搭載した状態を示す断面図、図17は前記半導体チップ1を搭載された可撓性配線基板2を折り曲げて前記半導体チップ1を積層する状態を示す図、図18は前記可撓性配線基板2の折り曲げ部で折り曲げてショートカット用配線を接続した状態の拡大断面図である。

【0034】図10～図18において、1は半導体チップ（ICチップ）、1Aは半導体チップの外部電極（パッド上のAuパンプ）、2は可撓性配線基板（フレキシブル配線基板）、2Aは折り曲げ部、3は配線、4はショートカット配線接続用Auパンプ、4Aはショートカット配線接続用ランド、5はビア、6は半導体チップ搭載用ランド、7は実装用半田ボール端子（共通配線外部端子）、9は実装基板、9Aは実装基板上の半導体装置実装用ランド、10は封止材、11はフレキシブル基板テープ、12は絶縁膜（保護膜）である。

【0035】まず、図12に示すような可撓性配線基板（フレキシブル配線基板）2を製造する。前記可撓性配線基板（フレキシブル配線基板）2の製造は、図12に示すように、フレキシブル基板テープ11の表主面（第1主面）に配線を形成し、その上に絶縁膜（保護膜）12を被覆する。この配線が形成されたフレキシブル基板テープ11の表主面に、半導体チップ1の同一機能の半導体チップ搭載用ランド6を接続する配線3、半導体チ

ップ1の同一機能の半導体チップ搭載用ランド6を接続するショートカット配線接続用ランド4Aとショートカット配線接続用Auパンプ4、前記配線3を通すビア5、及び半導体チップ搭載用ランド6をそれぞれ所定位置に形成する。前記フレキシブル基板テープ11の裏主面（第2主面）には、図13に示すように、半導体チップ1の同一機能の半導体チップ搭載用ランド6を接続する配線3ショートカット配線接続用ランド4A、及びショートカット配線接続用Auパンプ4並びに実装用半田ボール端子7を形成する。

【0036】本実施例2の半導体装置の製造方法は、前記図12に示すような可撓性配線基板（フレキシブル配線基板）2を用意する。次に、図14及び図15に示すように、前記可撓性配線基板2の表主面に所定の間隔で形成された半導体チップ搭載用ランド6上に複数の半導体チップ（ICチップ）1を搭載する。半導体チップ（ICチップ）1は、図16に示すように、半導体チップ搭載用ランド6と外部電極（パッド上のAuパンプ）1Aとを電気的に接続し、その接続部を封止材（封止樹脂）10で封止する。

【0037】前記複数の半導体チップ1が搭載された前記可撓性配線基板2の前記折り曲げ部2Aで折り曲げられて、図17に示すように、前記可撓性配線基板2の表主面に搭載された隣合の半導体チップ2が背中合わせに重ね合わせ、接着材（又は接着テープ）2Bで固定する。さらに、図17に示すように、前記可撓性配線基板2の前記折り曲げ部2Aで折り曲げて、ショートカット配線接続用Auパンプ4とショートカット配線接続用ランド4Aとを接続し、次の1組の積層体を積層する。このようにして複数組の積層体を構成する。

【0038】前記折り曲げ部の構成を図18（a）、（b）に示す。前記複数組の積層体の前記各積層体の同一機能の配線をショートカット配線部2Cで電気的に接続して前記可撓性配線基板2の配線長をショートカットして、図10に示すような半導体装置200を完成する。この半導体装置200は、図11に示すように、前記積層体の同一機能の配線の共通配線外部端子である実装用半田ボール端子7と実装基板9上の半導体装置実装用ランド9Aとを電気的に接続する。

【0039】以上説明したように、本実施例2によれば、折り曲げ可能な可撓性配線基板2を用い、前記各積層体の同一機能の配線をショートカット配線部で電気的に接続して、前記可撓性配線基板2の配線長をショートカットするので、配線長による信号遅延を防止することができる。また、配線基板を折り畳んで立体構造（三次元）にした半導体装置において、前記各積層体の同一機能の配線をショートカット配線部により積層体内部の熱の放熱効率を向上させることができる。また、実装用半田ボール端子部以外の基板の両面にICチップを両面実装することも可能である。

【0040】（実施例3）本発明の実施例3の半導体装置（300 or 400）は、前記実施例2と同様に前記実施例1のショートカット配線基板8を省略した別の実施例である。前記実施例1、2と同様にして、図19又は図20に示すような折り畳み構造にしたもの（300 or 400）である。この製造方法は、前記実施例1、2と同様にして製造することができる。

【0041】（実施例4）図21は本発明の実施例4の半導体装置の概要構成を示す平面図、横断面図及び縦断面図であり、図22は本実施例4の半導体装置を実装基板に実装した横断面図である。本実施例4の半導体装置は、図21に示すように、四つ折り曲げ部2Aを有するフレキシブル配線基板63の表主面（第1主面）に所定の間隔で複数の半導体チップ（ICメモリチップ）1が搭載され、前記フレキシブル配線基板63の前記折り曲げ部で二つ折りに曲げられて、前記フレキシブル配線基板63の表主面に搭載された隣合の半導体チップ1が背中合わせに重ね合わせられ、接着材（又は接着テープ）で固定される。さらに、前記フレキシブル配線基板63の前記四つ折り曲げ部で四つ折りに曲げられて、次の1組の積層体が積層される。このようにして複数組の積層体が構成される。該複数組の積層体の前記各積層体の同一機能の配線のショートカット配線接続用ランド61とショートカット配線接続用半田ボール端子62とを電気的に接続して前記フレキシブル配線基板63の配線長をショートカットされる。前記フレキシブル配線基板63の中央部には折り曲げストレス緩和用抜き穴26が設けられている。

【0042】本実施例4の半導体装置500は、図22に示すように、前記フレキシブル配線基板63の裏主面（第2主面）に設けられている実装用半田ボール端子（配線の共通端子）7と実装基板9の半導体装置実装用ランド9Aとを電気的に接続されて前記実装基板9に実装される。

【0043】次に、本実施例4の半導体装置の製造方法について説明する。図23は前記フレキシブル配線基板63の配線構成を示す表平面図、図24は前記フレキシブル配線基板63の配線構成を示す裏平面図、図25は前記フレキシブル配線基板63上に半導体チップ1を搭載した状態を示す全体平面図、図26は図25の側面図、図27は1個の半導体チップ1を前記フレキシブル配線基板63上に搭載した状態を示す断面図、図28は前記半導体チップ1を搭載されたフレキシブル配線基板63を二つ折りに曲げた平面図、横断面図、及び縦断面図、図29は前記半導体チップ1を搭載されたフレキシブル配線基板63を四つ折りに曲げた平面図である。

【0044】図21～図29において、1は半導体チップ（ICチップ）、1Aは半導体チップの外部電極（パッド上のAuパンプ）、2は配線、6は半導体チップ搭載用ランド、7は実装用半田ボール端子（共通配線外部

端子）、9は実装基板、9Aは実装基板上の半導体装置実装用ランド、10は封止材、12は絶縁膜（保護膜）、5はビア、17は微小（ビルドアップ）ビア、26は折曲げストレス緩和用抜き穴、61はショートカット接続配線用ランド、62はショートカット配線用半田ボール端子、63はポリイミドテープに配線を形成したフレキシブル配線基板（可撓性配線基板）である。

【0045】まず、図21に示すようなフレキシブル配線基板63を製造する。前記フレキシブル配線基板63の製造は、図23及び図24に示すように、フレキシブル配線基板63の配線を形成し、その上に絶縁膜（保護膜）を被覆する。このフレキシブル配線基板63の表主面（第1主面）に、半導体チップ1の同一機能の半導体チップ搭載用ランドを接続する配線3、半導体チップ1の同一機能の半導体チップ搭載用ランドを接続するショートカット配線接続用ランド61、ショートカット配線用半田ボール端子62パンプ、及び半導体チップ搭載用ランド6をそれぞれ所定位置に形成する。前記フレキシブル配線基板63の裏主面（第2主面）には、図24に示すように、半導体チップ1の同一機能の半導体チップ搭載用ランドを接続する配線3、ショートカット配線接続用ランド61、及びショートカット配線接続用Auパンプ62、並びに実装用半田ボール端子7を形成する。

【0046】本実施例4の半導体装置の製造方法は、前記図23及び図24に示すようなフレキシブル配線基板63を用意する。次に、図25及び図26に示すように、前記フレキシブル配線基板63の表主面に所定の間隔で形成された半導体チップ搭載用ランド上に複数の半導体チップ（ICチップ）1を搭載する。半導体チップ（ICチップ）1は、図27に示すように、半導体チップ搭載用ランドと外部電極（パッド上のAuパンプ）1Aとを電気的に接続し、その接続部を封止材（封止樹脂）で封止する。

【0047】また、多層配線を必要とされる場合は、前記図27に示すように、フレキシブル配線基板63にビルドアップ方式等を部分的に使用することで、高度な配線の可能な多層配線部（図左端より中央部右の最も薄い部分手前まで及び右端の厚くなっている部分）と片面あるいは両面の単層配線で折り曲げ可能な部位（前記多層配線部に挟まれた最も薄い部分）の共存するフレキシブル配線基板63が作成可能となる。

【0048】前記複数の半導体チップ1が搭載された前記フレキシブル配線基板63の前記折り曲げ部2Aで二つ折りに曲げられて、図28に示すように、前記フレキシブル配線基板63の表主面に搭載された隣合の半導体チップ1が背中合わせに重ね合わせ、接着材（又は接着テープ）で固定する。さらに、図29に示すように、前記フレキシブル配線基板63の前記折り曲げ部2Aで四つ折りに曲げて、次の1組の積層体を積層する。このようにして前記図21に示すような半導体チップ1が背中

合わせに重ね合わせた複数組の積層体を構成する。前記複数組の積層体の前記各積層体の同一機能の配線をショートカットさせる短絡電極で電氣的に接続して前記フレキシブル配線基板63の配線長をショートカットする。

【0049】本実施例4の半導体装置500は、図22に示すように、前記フレキシブル配線基板63の裏主面（第2主面）に設けられている共通端子である実装用外部電極7と実装基板9の半導体装置実装用ランド9Aとを電氣的に接続して前記実装基板9に実装される。なお、折曲げストレスが大きくない場合は折り曲げストレス緩和用抜き穴26を設けなくてもよい。また、実装用半田ボール端子部以外の基板の両面にICチップを両面実装することも可能である。

【0050】（実施例5）図30は本発明の実施例5の半導体装置の吸熱パッドをパッケージ内に収納した状態の概要構成を示す断面図、図31は図30の吸熱パッドをパッケージ内に収納した状態の概要構成を示す平面図、図32は図30の吸熱パッドによる冷却機構の概要構成を示す模式図である。

【0051】図30～図32において、1は半導体チップ（ICチップ）、1Aは半導体チップの外部電極（パッド上のAuパンプ）、7は実装用半田ボール端子（共通配線外部端子）、26は折曲げストレス緩和用抜き穴、61はショートカット配線接続用ランド、62はショートカット配線接続用半田ボール端子、63はポリイミドテープ（フレキシブル基板）、64は吸熱パッド、65はパイプ、66は水路、67はファン、68は放熱部（ラジエーター）、69は放熱フィン、70は冷却液循環ポンプ、71は折り畳み積層パッケージ、72は熱伝導接着テープである。

【0052】本発明の実施例5の半導体装置は、前記実施例のような蛇腹折りや二つ折り、三つ折りの以外に十字折りのある折曲げ積層化ができる例であり、図30及び図31に示すように、フレキシブル配線基板63（可撓性配線基板）を四つ折りにして半導体チップ1を積層するものである。そして、十字に折られてストレスの集中するフレキシブル配線基板63の中央部に折り曲げストレス緩和用抜き穴26が設けられたものである。

【0053】すなわち、四つ折り曲げ部と中央部に折り曲げストレス緩和用抜き穴26を有し、複数の半導体チップ1が表面に所定の間隔で搭載可能なフレキシブル配線基板63と、該フレキシブル配線基板63の前記二つ折り曲部で折り曲げられて前記フレキシブル配線基板63の表面に搭載された半導体チップ1が背中合わせで重ね合わされた複数組の積層体とを備えた半導体装置であって、前記フレキシブル配線基板63の表主面に所定位置に複数の半導体チップ（ICメモリチップ）1が搭載され、前記可撓性配線基板2の前記折り曲部2Aで四つ折りに曲げられて、前記フレキシブル配線基板63の表主面に搭載された半導体チップ1が背中合わせに重ね合

わされ、接着材（又は接着テープ）2Bで固定される。さらに、前記フレキシブル配線基板63の前記折り曲部2Aで四つ折り曲げられて、次の1組の積層体が積層されている。このようにして複数組の積層体が構成されている。

【0054】前記フレキシブル配線基板63に用いられる可撓性テープ基材の厚さは、例えば、75 $\mu$ m、Cu配線の厚さは35 $\mu$ mである。該複数組の積層体の前記各積層体の同一機能の配線をショートカットさせる短絡電極で電氣的に接続して前記フレキシブル配線基板63の配線長をショートカットする。

【0055】また、図30及び図31に示すように、前記半導体チップが重ね合わされた積層体間に吸熱パッド（冷却路）64が設けられている。前記吸熱パッド（冷却路）64は、図30及び図31に示すように、水路66が形成されたものである。この吸熱パッド（冷却路）64は、折り畳み積層パッケージ71の前記半導体チップが重ね合わされた積層体間に、熱伝導接着テープ72により固定されている。

【0056】また、前記吸熱パッド64は、ICパッケージ等を使用される絶縁セラミックス等の内部に水路66を持つものである。前記水路66はパイプ65を通じて放熱部68につながっており、内部は水等の液体を充填してある。吸熱パッド64の取り付けには熱伝導接着テープ72を使用するが、より高性能を狙ってシリコングリス+接合材を使用してもよい。冷却液循環ポンプ70で強制的に内部の液体を循環させ、吸熱パッド64で吸収した熱を循環する液体を媒介してパイプ65を通して放熱部68に送りファン67で強制冷却する。放熱部68で冷された液体はパイプ65を通して再び吸熱パッド64に送られる。他にもヒートパイプや放熱板等を挟み込んだり、ヒートシンクを取り付けることもよい。

【0057】また、多層配線を必要とされる場合は、前述した図27に示すようにして、フレキシブル配線基板63にビルドアップ方式等を部分的に使用することで、高度な配線の可能な多層配線部（図左端より中央部右の最も薄い部分手前まで及び右端の厚くなっている部分）と片面あるいは両面の単層配線で折り曲げ可能な部位（前記多層配線部に挟まれた最も薄い部分）の共存するフレキシブル配線基板63を作成する。

【0058】前記ビルドアップ多層配線部は、ポリイミドテープ（フレキシブル基板）63の上に銅等の導電性物質で配線3を作り、絶縁感光性樹脂18を積み、露光により微小（ビルドアップ）ビア17を開けながら他の部分を硬化させ絶縁層として上に銅等の導電性物質で配線3を作りこんでいくため、単層配線で折り曲げ可能な部位も微小（ビルドアップ）ビア17と同様の方法で製造可能となる。

【0059】実施例1～5では、Auパンプによるベアチップ実装による製造方法で説明しているが、他にワイ

ヤーボンディングやビームリード等他の製造方法も可能なのは言うまでもない。また、前記実施例では半導体装置及びその製造方法について説明したが、本発明は、半導体モジュール及びその製造方法にも適用できることは前記説明から明らかである。

【0060】以上、本発明を、前記実施例に基づき具体的に説明したが、本発明は、前記実施例に限定されるものではなく、その要旨を逸脱しない範囲において種々変更可能であることは勿論である。

【0061】

【発明の効果】本願において開示される発明によって得られる効果を簡単に説明すれば、以下のとおりである。本願発明によれば、可撓性配線基板を折り畳んで立体構造（三次元）にした半導体装置もしくは半導体モジュールにおいて、配線をショートカットさせる短絡電極で電氣的に接続して配線長をショートカットするので、配線長による信号遅延を防止することができる。また、前記半導体チップが重ね合わされた積層体間に吸熱パッド（冷却路）が設けられているので、放熱効率を向上することができる。

【図面の簡単な説明】

【図 1】本発明の実施例 1 の半導体装置の概要構成を示す正面図である。

【図 2】本実施例 1 の半導体装置を実装基板に実装した正面図である。

【図 3】本実施例 1 の可撓性配線基板の配線構成を示す表平面図である。

【図 4】本実施例 1 の可撓性配線基板の配線構成を示す裏平面図である。

【図 5】本実施例 1 の可撓性配線基板上に半導体チップを搭載した状態を示す全体平面図である。

【図 6】図 5 の側面図である。

【図 7】本実施例 1 の 1 個の半導体チップを可撓性配線基板上に搭載した状態を示す断面図である。

【図 8】本実施例 1 のショートカット配線基板の一方の配線基板と他方の配線基板の配線構成を示す平面図である。

【図 9】本実施例 1 のショートカット配線基板の一方の配線基板を可撓性配線基板の配線に接続した状態を示す図である。

【図 10】本発明の実施例 2 の半導体装置の概要構成を示す正面図である。

【図 11】本実施例 2 の半導体装置を実装基板に実装した正面図である。

【図 12】本実施例 2 の可撓性配線基板 2 の配線構成を示す表平面図である。

【図 13】本実施例 2 の可撓性配線基板の配線構成を示す裏平面図である。

【図 14】本実施例 2 の可撓性配線基板上に半導体チップを搭載した状態を示す全体平面図である。

【図 15】図 14 の側面図である。

【図 16】本実施例 2 の 1 個の半導体チップ可撓性配線基板上に搭載した状態を示す断面図である。

【図 17】本実施例 2 の半導体チップを搭載された可撓性配線基板を折り曲げて半導体チップを積層する状態を示す図である。

【図 18】本実施例 2 の可撓性配線基板の折り曲げ部で折り曲げてショートカット用配線を接続した状態の拡大断面図である。

【図 19】本発明の実施例 3 の半導体装置の概要構成を示す正面図、平面図及び側面図である。

【図 20】本発明の実施例 3 の半導体装置の概要構成を示す正面図である。

【図 21】本発明の実施例 4 の半導体装置の概要構成を示す平面図、横断面図及び縦断面図である。

【図 22】本実施例 4 の半導体装置を実装基板に実装した横断面図である。

【図 23】本実施例 4 の可撓性配線基板の配線構成を示す表平面図である。

【図 24】本実施例 4 の可撓性配線基板の配線構成を示す裏平面図である。

【図 25】本実施例 4 の可撓性配線基板上に半導体チップを搭載した状態を示す全体平面図である。

【図 26】図 25 の側面図である。

【図 27】本実施例 4 の 1 個の半導体チップを前記可撓性配線基板上に搭載した状態を示す断面図（多層配線使用時のもの）である。

【図 28】本実施例 4 の半導体チップを搭載された可撓性配線基板を二つ折りに曲げた平面図、横断面図、及び縦断面図である。

【図 29】本実施例 4 の半導体チップを搭載された可撓性配線基板を四つ折りに曲げた平面図である。

【図 30】本発明の実施例 5 の半導体装置の吸熱パッドをパッケージ内に収納した状態の概要構成を示す断面図である。

【図 31】本実施例 5 の吸熱パッドをパッケージ内に収納した状態の概要構成を示す平面図である。

【図 32】本実施例 5 の吸熱パッドによる冷却機構の概要構成を示す模式図である。

【符号の説明】

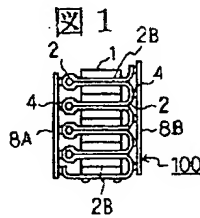
- |                    |                     |
|--------------------|---------------------|
| 1…半導体チップ（ICチップ）    | 1A…半導体チップの外部電極      |
| 2…可撓性配線基板          | 2A…折り曲部             |
| 2B…半導体チップ接着剤       | 2C…ショートカット配線接続部     |
| 3…配線               | 4…ショートカット配線接続用Auパンプ |
| 4A…ショートカット配線接続用ランド | 5…ビア                |
|                    | 6…半導体チップ搭載用ランド      |

7…実装用半田ボール端子  
 ートカット配線基板  
 9…実装基板  
 実装用ランド  
 10…封止材  
 ル基板テープ  
 12…絶縁膜（保護膜  
 ドアップ）ビア  
 18…絶縁感光性樹脂  
 23…半田

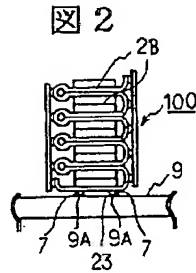
8 A, 8 B…ショ  
 9 A…半導体装置  
 11…フレキシブ  
 17…微小（ビル  
 22…接着テープ  
 26…折曲げスト

レス緩和抜き穴  
 61…ショートカット配線接続用ランド  
 62…ショートカット配線用半田ボール端子  
 63…フレキシブル配線基板  
 64…吸熱パット  
 65…パイプ  
 66…水路  
 67…ファン  
 68…放熱部（ラジエター）  
 69…放熱フィン  
 70…冷却液循環ポンプ  
 71…折り畳み積  
 層パッケージ  
 72…熱伝導接着テープ

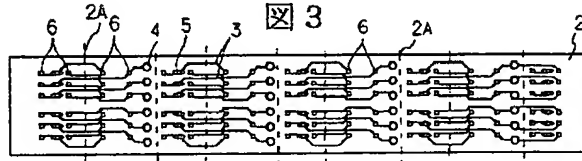
【図1】



【図2】

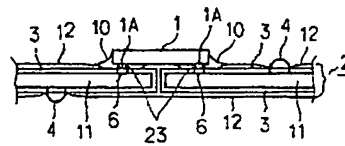


【図3】



【図7】

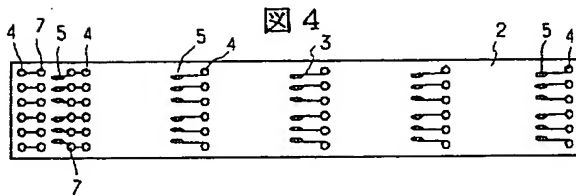
図7



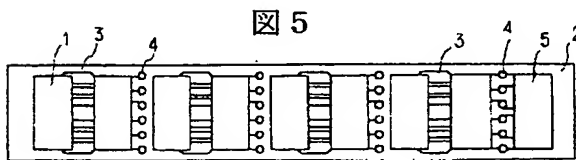
【図8】

図8

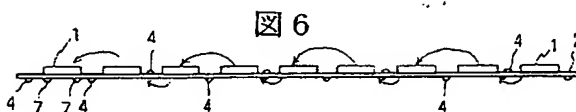
【図4】



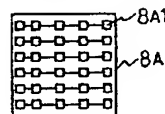
【図5】



【図6】

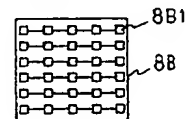


(a)



【図9】

(b)



【図10】

図9

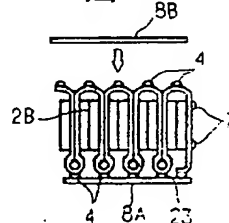
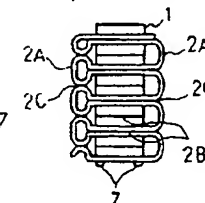
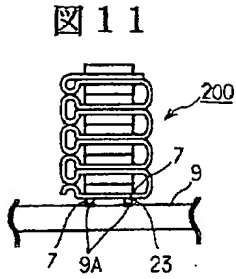


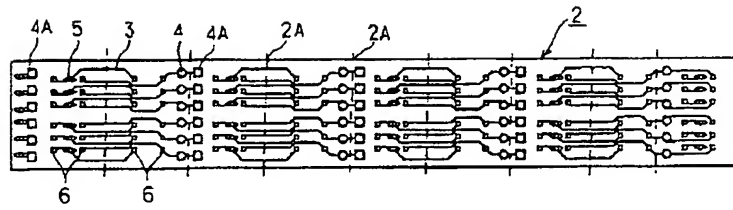
図10



【図11】

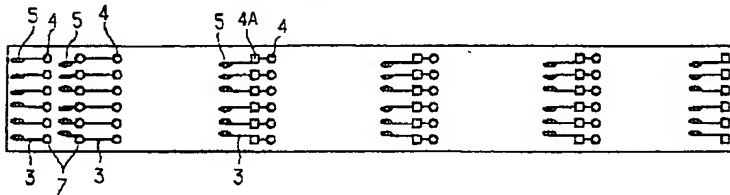


【図12】



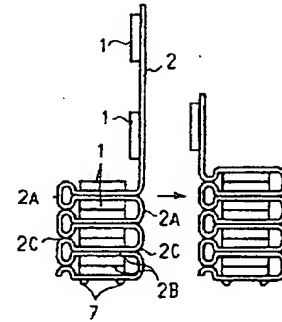
【図13】

図13



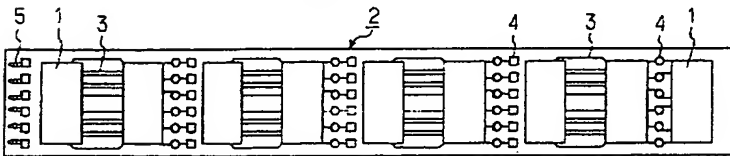
【図17】

図17



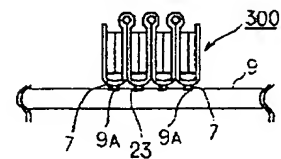
【図14】

図14



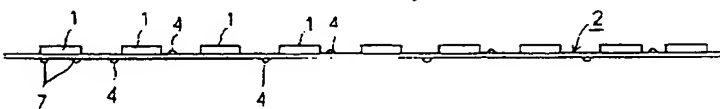
【図19】

図19



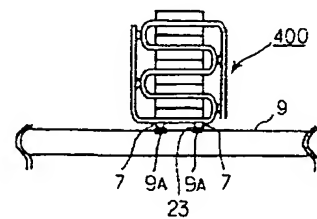
【図15】

図15



【図20】

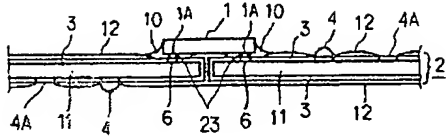
図20





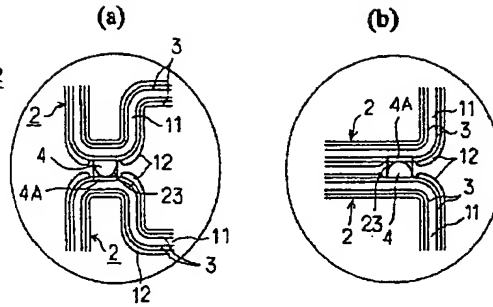
【図16】

図16



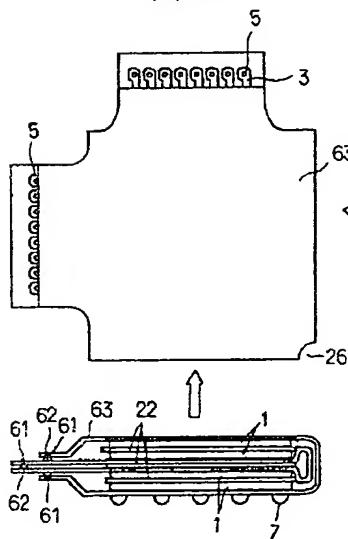
【図18】

図18



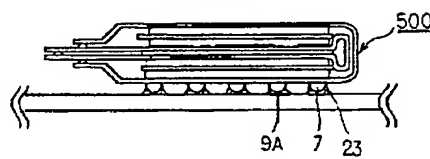
【図21】

図21



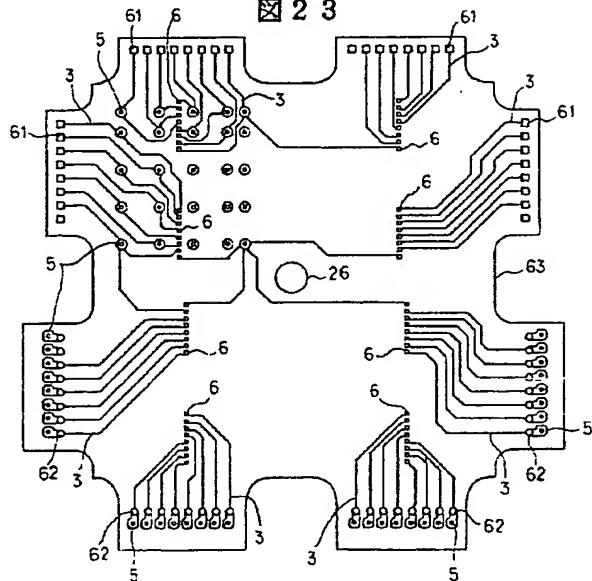
【図22】

図22



【図23】

図23



【図26】

図26

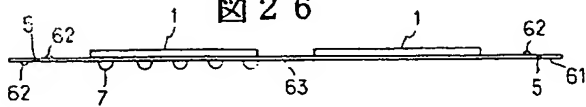


图 24

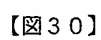
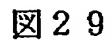
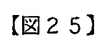


图 30

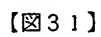
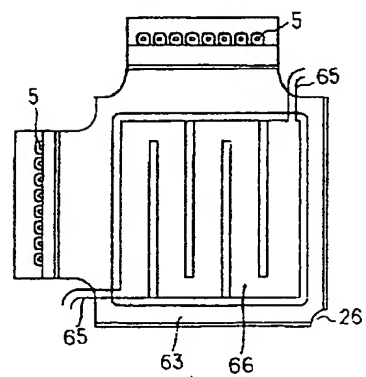
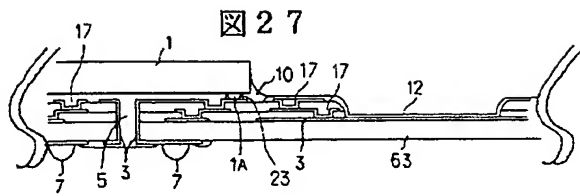


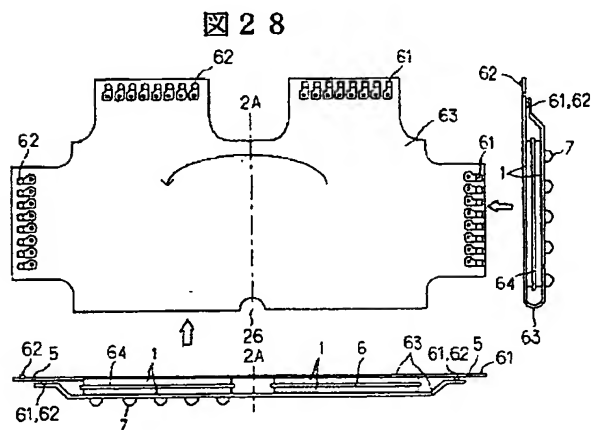
图 3 1



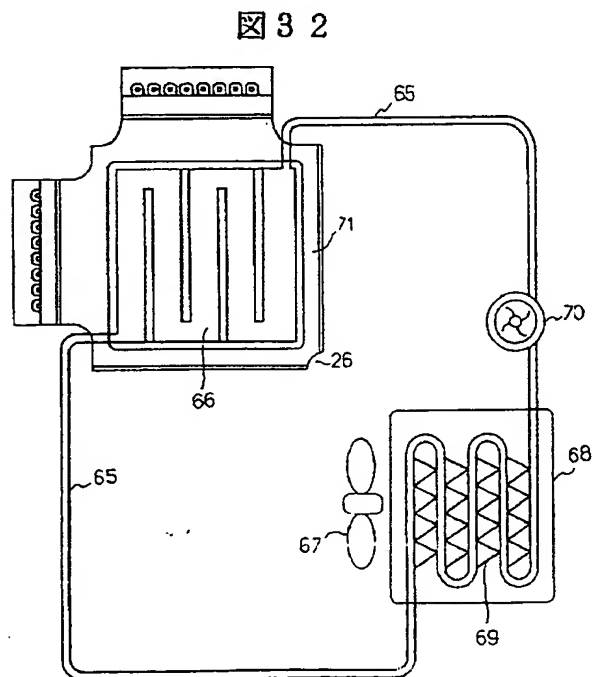
【図27】



【図28】



【図32】



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 5E344 BB02 BB03 BB04 CC25 DD16  
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 5F036 AA01 BB21 BB35 BB43 BC05  
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SEMICONDUCTOR DEVICE, METHOD OF MANUFACTURING SAME, AND  
SEMICONDUCTOR MOUNTING METHOD

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[There are no amendments to this patent.]

### Abstract

#### Purpose

To prevent signal delay due to wiring length in a semiconductor device or semiconductor module having a three-dimensional (3-dimensional) structure by folding up a flexible wiring board. To increase the heat dissipation efficiency.

#### Constitution

A type of semiconductor device or semiconductor module characterized by the following facts: it has a flexible wiring board that has folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, and at least one set of laminates created by folding said flexible wiring board at said folding portions and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board; wirings having the same function of the laminates are electrically connected by shortcut wiring boards.

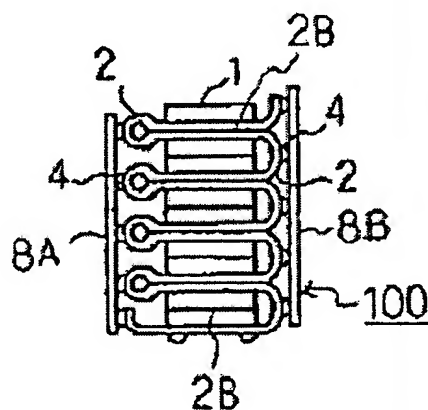


Figure 1

### Claims

1. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding said flexible wiring board at said double folding portions and thereby superposing adjacent

semiconductor chips mounted on said first principal surface of said flexible wiring board, and shortcut wiring boards that electrically connect wirings having the same function of the laminates.

2. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding said flexible wiring board at said double folding portions and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the laminates, common terminals for the wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board, and a means for forming an electrical connection between the common terminals and the wiring lands of the mounting substrate.

3. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions being sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; and a step in which wirings having the same function of said laminates are electrically connected with shortcut wiring boards.

4. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed, and which has common terminals for wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that adjacent semiconductor chips

mounted on the first principal surface of said flexible wiring board are superposed and laminated; a step in which wirings having the same function of said laminates are electrically connected with shortcut wiring boards; and a step in which electrical connection is made between said common terminals and the wiring lands of the mounting substrate.

5. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding said flexible wiring board at said double folding portions and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring shortcuts.

6. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding said flexible wiring board at said double folding portions and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the laminates, connecting portions that electrically connect wirings having the same function of said laminates to create wirings shortcuts, common terminals for the wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board, and a means that electrically connects the common terminals and the wiring lands of the mounting substrate.

7. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed and connecting portions for shortcut wirings that create shortcut for wirings having the same function of said laminates; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; and a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts.

8. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed, and that has common terminals for wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; a step in which electrical connection of wirings having the same function of said laminates is made to create wiring shortcuts; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the wiring lands of the mounting substrate.

9. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has quarter folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring shortcuts.

10. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has quarter folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the laminates, connecting portions that electrically connect wirings having the same function of said laminates to create wiring shortcuts, common terminals for the wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board, and a means that electrically connects the common terminals and the wiring lands of the mounting substrate.

11. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter

folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed when folding at said quarter folding portions, and connecting portions for the wirings having the same function of said laminates to create wiring shortcuts ; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; and a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts.

12. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed when folding at said quarter folding portions, and that has common terminals for wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the lands of the mounting substrate.

13. A type of semiconductor device characterized by the following facts: it has a flexible wiring board that has quarter folding portions or double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions or double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring shortcuts; and a cooling path is provided between laminates with said superposed semiconductor chips.

14. A type of semiconductor device characterized by the following facts: it has a flexible wiring board that has quarter folding portions or double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, and at least one set of laminates created by folding at said quarter folding portions or double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board; the lands for shortcut wiring for wirings having the same function of said laminates are electrically connected, and electrical connection is made between the common terminals of the wirings having the same function of said laminates and the lands on the mounting substrate; in this semiconductor device, a cooling path is provided between the laminates with said superposed semiconductor chips; common terminals having the same function of said laminates are arranged on the second principal surface of said flexible wiring board; and electrical connection is made between said common terminals and the wiring lands of the mounting substrate.

15. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions or double folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed when folding at said quarter folding portions and double folding portions, and connecting portions for wirings having the same function of said laminates to create wiring shortcuts; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions or double folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; a step in which a cooling path is formed by means of thermoconductive adhesive tape and heat absorptive pads between said laminates with said superposed semiconductor chips; a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts.

16. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions or double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed when said quarter folding portions or double folding portions are folded, and which has common terminals for wirings having the same function of said laminates arranged on the second principal surface



of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said [quarter folding portions or] double folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the lands of the mounting substrate.

#### Detailed explanation of the invention

[0001]

##### Technical field of the invention

The present invention pertains to a surface-mount type of semiconductor device or semiconductor module, and its manufacturing method. In particular, the present invention pertains to an effective technology in which plural semiconductor chips are mounted on a flexible wiring board (flexible wiring substrate) or a leadframe, and the adjacent semiconductor chips, that is, said mounted semiconductor chips, are attached back-to-back, and laminated.

[0002]

##### Prior art

As a semiconductor device of small size with a and high degree of integration, for example, Japanese Kokai Patent Application No. Hei 9[1997]-181215 proposed a type of semiconductor device characterized by the following facts: there is a package for assembling semiconductor chips in the stacked portions of a flexible wiring board (flexible wiring substrate), and there is also a package (sealed body) for mounting semiconductor chips on the side opposite the side where the external terminals for mounting semiconductor chips (lands for mounting semiconductor chips) on the flexible wiring board are positioned (see: Figures 22-24).

[0003]

##### Problems to be solved by the invention

After studying the aforementioned prior art, the present inventors have found the following problems. Although said prior art can realize a three-dimensional (3-D) structure with a small footprint and a high degree of integration, it has only a folded planar (two-dimensional) board as the substrate, so that the wiring length is the same as that in the conventional planar

board constitution. Consequently, the problem of signal delay due to the wiring length exists. Also, due to stacking of plural semiconductor chips (IC chips) in a narrow space, it is difficult for the heat generated in the package to dissipate, and defective operation may result. This is undesirable. Also, the solder ball terminals of the BGA (Ball Grid Array) cannot deform differently from the lead terminals, so that cracks or breakage may occur due to deformation or expansion of the mounting substrate.

[0004]

The purpose of the present invention is to provide a technology that can prevent signal delay due to wiring in the semiconductor device or semiconductor module in a three-dimensional (3-D) structure created by folding the board. Another purpose of the present invention is to provide a technology that can increase the heat dissipation efficiency of the semiconductor device or semiconductor module in a three-dimensional (3D) structure created by folding the board. The aforementioned and other purposes, as well as other novel features of the present invention, will be explained in the description and appended figures of the present specification.

[0005]

Means to solve the problems

In the following, a brief account will be presented for the inventions described in the present patent application. The first invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, and shortcut wiring boards that electrically connect wirings having the same function of the laminates.

[0006]

The second invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the

laminates, common terminals for the wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board, and a means for forming an electrical connection between the common terminals and the wiring lands of the mounting substrate.

[0007]

The third invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; and a step in which wirings having the same function of said laminates are electrically connected with shortcut wiring boards.

[0008]

The fourth invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed, and which has common terminals for wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board; a step in which electrical connection is made between the lands for mounting plural groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; a step in which wirings having the same function of said laminates

are electrically connected with shortcut wiring boards; and a step in which electrical connection is made between said common terminals and the wiring lands of the mounting substrate.

[0009]

The fifth invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring for shortcuts.

[0010]

The sixth invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the laminates, connecting portions that electrically connect wirings having the same function of said laminates to create wiring shortcuts, common terminals for the wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board, and a means that electrically connects the common terminals and the wiring lands of the mounting substrate.

[0011]

The seventh invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed and connecting portions of wirings for shortcuts that make shortcuts for the wirings having the same function of said laminates; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads)

of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; and a step in which electrical connection of wirings having the same function of said laminates is made to create wiring shortcuts.

[0012]

The eighth invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed, and which has common terminals for wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; a step in which electrical connection is made to create wiring shortcuts for the wirings having the same function of said laminates; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the wiring lands of the mounting substrate.

[0013]

The ninth invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has quarter folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring shortcuts.

[0014]

The tenth invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has quarter folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the laminates, connecting portions that electrically connect wirings having the same function of said laminates to create wiring shortcuts, common terminals of the wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board, and a means that electrically connects the common terminals and the wiring lands of the mounting substrate.

[0015]

The eleventh invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed when folding at said quarter folding portions, and connecting portions for wirings having the same function of said laminates to create wiring shortcuts; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; and a step in which electrical connection is made for wirings having the same function of said laminates to create shortcuts.

[0016]

The twelfth invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are



superposed when folding at said quarter folding portions, and which has common terminals of wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the lands of the mounting substrate.

[0017]

The thirteenth invention provides a type of semiconductor device characterized by the following facts: it has a flexible wiring board that has quarter folding portions or double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions or double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring shortcuts; and a cooling path is provided between laminates with said superposed semiconductor chips.

[0018]

The fourteenth invention provides a type of semiconductor device characterized by the following facts: it has a flexible wiring board that has quarter folding portions or double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, and at least one set of laminates created by folding at said quarter folding portions or double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board; the lands for shortcut wiring for wirings having the same function of said laminates are electrically connected, and electrical connection is made between the common terminals of the wirings having the same function of said laminates and the lands on the mounting substrate; in this semiconductor device, a cooling path is provided between the laminates with said superposed semiconductor chips; common terminals having the

same function of said laminates are arranged on the second principal surface (inner principal surface) of said flexible wiring board; and electrical connection is made between said common terminals and the wiring lands of the mounting substrate.

[0019]

The fifteenth invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions or double folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed when folding at said quarter folding portions and double folding portions, and connecting portions for wirings having the same function of said laminates to create wiring shortcuts, is prepared; a step in which electrical connection is made between the lands for mounting plural groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions or double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; a step in which a cooling path is formed by means of thermoconductive adhesive tape and heat absorptive pads between said laminates with said superposed semiconductor chips; a step in which electrical connection is made for wirings having the same function of said laminates to create the wiring shortcuts.

[0020]

The sixteenth invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions or double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed when said quarter folding portions or double folding portions are folded, and which has common terminals for wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board; a step in which electrical connection is made between the lands for mounting plural groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible

wiring board is folded at said [quarter folding portions or] double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the lands of the mounting substrate.

[0021]

#### Embodiments of the invention

In the following, an explanation will be given in detail regarding the embodiments (Application Examples) of the present invention, with reference to figures. The same part numbers are adopted throughout all of the figures used to illustrate the application examples, and they will not be explained repeatedly.

[0022]

#### Application Example 1

Figure 1 is a schematic front view illustrating the constitution of the semiconductor device in Application Example 1 of the present invention. Figure 2 is a front view illustrating the state in which the semiconductor device of Application Example 1 is mounted on a mounting substrate. As shown in Figure 1, in the semiconductor device of Application Example 1, plural semiconductor chips (IC chips) (1) are mounted at a prescribed interval on the outer principal surface (first principal surface) of flexible wiring board (2) having double folding portions. When said flexible wiring board (2) is folded at said double folding portions, adjacent semiconductor chips (1) mounted on the outer principal surface of said flexible wiring board (2) are superposed back-to-back, and adhesive (or adhesive tape) (2B) is used to fix them together. In addition, said flexible wiring board (2) is folded at said double folding portions (2A), and the next set of laminates are layered. In this way, plural sets of laminates are formed. Wiring with the same function of said laminates of said plural sets of laminates are electrically connected with shortcut wiring board (8) to reduce the wiring length of said flexible wiring board (2). Said flexible wiring board (2) has a thickness of, for example, 75  $\mu\text{m}$ , and the Cu wiring has a thickness of, for example, 35  $\mu\text{m}$ .

[0023]

As shown in Figure 2, for semiconductor device (100) of Application Example 1, electrical connection is made between mounting solder ball terminals (common wiring terminals) (7) provided on the inner principal surface (second principal surface) of said flexible wiring

board (2) and lands (9A) for semiconductor device mounting on mounting substrate (9), so that the semiconductor device is mounted on said mounting substrate (9).

[0024]

In the following, an explanation will be given regarding the method of manufacturing the semiconductor device in Application Example 1. Figure 3 is a outer plan view illustrating the wiring constitution of said flexible wiring board (2). Figure 4 is an inner plan view illustrating the wiring constitution of said flexible wiring board (2). Figure 5 is an overall plan view illustrating the state in which semiconductor chips (1) are mounted on said flexible wiring board (2). Figure 6 is a side view of Figure 5. Figure 7 is a cross section illustrating the state in which one semiconductor chip (1) is mounted on said flexible wiring board (2). Figure 8 is a plan view illustrating the wiring constitution of wiring board (8A) as one of said shortcut wiring boards (8A), (8B), and of the other wiring board (8B). Figure 9 is a diagram illustrating the state in which wiring board (8A), one of said shortcut wiring boards (8A), (8B), is connected to the wiring of said flexible wiring board (2).

[0025]

In Figures 3-9, (1) represents semiconductor chips (IC chips); (1A) represents the external electrodes of the semiconductor chips (Au bumps on the pads); (2) represents the flexible wiring board (flexible wiring substrate); (2A) represents the double folding portions; (3) represents wiring; (4) represents Au bumps for connection of shortcut wiring; (5) represents via; (6) represents lands for mounting the semiconductor chips; (7) represents solder ball terminals for mounting (external common wiring terminals); (8A), (8B) represent shortcut wiring boards; (8A1), (8B1) represent shortcut wiring lands; (9) represents a mounting substrate; (9A) represents lands for mounting of semiconductor device on the mounting substrate; (10) represents a sealant; (11) represents flexible board tape; and (12) represents an insulating film (protective film).

[0026]

First of all, flexible wiring board (flexible wiring substrate) (2) is manufactured as shown in Figure 3. As shown in Figure 3, when said flexible wiring board (flexible wiring substrate) (2) is manufactured, wiring is formed on flexible substrate tape (11), with insulating film (protective film) (12) covering it. On the outer principal surface of flexible substrate tape (11) with wiring formed on it as described, wiring (3) for connecting lands (6) for mounting semiconductor chips that have the same function on semiconductor chips (1), Au bumps (4) for shortcut wiring connection that connect lands (6) for mounting semiconductor chips that have the same function

on semiconductor chips (1), via (5) to let said wiring (3) pass through, and lands (6) for mounting semiconductor chips are formed at their respective positions. as shown in Figure 4, wiring (3) for connecting lands (6) for mounting semiconductor chips that have the same function on semiconductor chips (1), as well as Au bumps (4) for shortcut wiring connection and solder ball terminals (external common wiring terminals) (7) for mounting are formed on the inner principal surface of said flexible substrate tape (11).

[0027]

In the method of manufacturing the semiconductor device in Application Example 1, as shown in said Figure 3, a flexible wiring board (flexible wiring substrate) (2) is prepared. Then, as shown in Figures 5 and 6, external electrodes of the semiconductor chips (Au bumps on the pads) (1A) are electrically connected with lands (6), which are for mounting semiconductor chips and are formed at a prescribed interval on the outer principal surface of said flexible wiring board (2), in order to mount plural semiconductor chips (IC chips) (1). That is, as shown in Figure 7, for semiconductor chips (IC chips) (1), external electrodes (Au bumps on the pads) (1A) and lands (6) for mounting the semiconductor chips, are electrically connected, followed by sealing of the connection region with sealant (sealing resin) (10).

[0028]

As shown in Figure 6, said flexible wiring board (2) having said plural semiconductor chips (1) mounted on it is folded at said double folding portions (2A) in the direction indicated by arrows. As a result, adjacent semiconductor chips (1) mounted on the outer principal surface of said flexible wiring board (2) are superposed back-to-back, and they are fixed together with adhesive (or adhesive tape) (2B). Said flexible wiring board (2) is further folded at said double folding portions (2A), Au bumps (4) for shortcut wiring connection and lands (4A) for shortcut wiring connection are [electrically] connected, and the next sets of laminates are layered on. In this way, plural sets of laminates are formed.

[0029]

As shown in Figure 9, first of all, by means of shortcut wiring board (8A) shown in Figure 8(a), wirings having the same functions of said laminates of said plural sets of laminates are electrically connected to Au bumps (4) for shortcut wiring connection of wirings having the same function on the left side of the laminates. Then, shortcut wiring lands (8B1) of shortcut wiring board (8B) shown in Figure 8(b) are electrically connected to Au bumps (4) for shortcut wiring connection of wirings having the same function on the right side of the laminates. As a result, the wiring length of said flexible wiring board (2) can be reduced. As shown in Figure 1,

semiconductor device (100) is completed in this way. As shown in Figure 2, in said semiconductor device (100) electrical connection is performed between solder ball terminals for mounting (common wiring terminals) (7), as the common terminals for wirings of the laminates having the same function, and lands (9A) on mounting substrate (9) for semiconductor device assembly.

[0030]

As explained above, according to Application Example 1, flexible wiring board (2) that can be folded enables electrical connection to be performed for wirings of the laminates having the same function by means of shortcut wiring boards (8A), (8B), and the wiring length of said flexible wiring board (2) is reduced. Consequently, it is possible to prevent signal delay due to the wiring length. Also, in a semiconductor device having a three-dimensional (3D) structure created by folding the wiring board, it is possible to increase the efficiency of heat dissipation for heat generated inside the laminates by means of shortcut wiring boards (8A), (8B) for said wirings having the same function of the laminates. Also, it is possible to realize double-sided assembly of IC chips on both surfaces of the board, rather than at the solder ball terminal regions for mounting.

[0031]

#### Application Example 2

Figure 10 is a front view illustrating schematically the constitution of the semiconductor device of Application Example 2 of the present invention. Figure 11 is a front view of the semiconductor device of Application Example 2 mounted on the mounting substrate. The semiconductor device in Application Example 2 is an application example in which the shortcut wiring boards (8A), (8B) of said Application Example 1 are omitted. That is, as shown in Figure 10, said flexible wiring board (2) having said plural semiconductor chips (IC chips) (1) mounted on it at prescribed intervals on the outer principal surface of said flexible wiring board (2) having folding portions (2A) is folded at said double folding portions (2A). As a result, adjacent semiconductor chips (2) mounted on the outer principal surface (first principal surface) of said flexible wiring board (2) are superposed back-to-back, and they are fixed together with adhesive (or adhesive tape) (2B). Said flexible wiring board (2) is further folded at said double folding portions (2A), Au bumps (4) for shortcut wiring connection and lands (4A) for shortcut wiring connection are connected, and the next sets of laminates are layered on. In this way, plural sets of laminates are formed. Said lands (4A) for shortcut wiring connection of wirings having the same function of the laminates and Au bumps (4) for shortcut wiring connection of

the wirings having the same function of the laminates of said plural sets of laminates are electrically connected to reduce the wiring length of said flexible wiring board (2).

[0032]

As shown in Figure 11, in semiconductor device (200) of Application Example 2, solder ball terminals for mounting (common wiring terminals) (7) provided on the inner principal surface (second principal surface) of said flexible wiring board (2) and lands (9A) on assembly substrate (9) for semiconductor device mounting are electrically connected in mounting said device on said mounting substrate (9).

[0033]

In the following, an explanation will be given regarding the method of manufacturing the semiconductor device in Application Example 2. Figure 12 is an outer plan view illustrating the wiring constitution of said flexible wiring board (2). Figure 13 is an inner plan view illustrating the wiring constitution of said flexible wiring board (2). Figure 14 is an overall plan view illustrating the state in which semiconductor chips (1) are mounted on said flexible wiring board (2). Figure 15 is a side view of Figure 14. Figure 16 is a cross section illustrating the state in which one semiconductor chip (1) is mounted on the outer principal surface of said flexible wiring board (2). Figure 17 is a diagram illustrating the state in which flexible wiring board (2) with said semiconductor chips (1) mounting on it is folded to stack said semiconductor chips (1). Figure 18 is an enlarged cross section illustrating the state of connection of the shortcut wiring by folding said flexible wiring board (2) at the double folding portions.

[0034]

In Figures 10-18, (1) represents semiconductor chips (IC chips); (1A) represents the external electrodes of the semiconductor chips (Au bumps on the pads); (2) represents the flexible wiring board (flexible wiring substrate); (2A) represents the double folding portions; (3) represents wiring; (4) represents Au bumps for shortcut wiring connection; 4A represents lands for the shortcut wiring connection; (5) represents via; (6) represents lands for mounting the semiconductor chips; (7) represents solder ball terminals for mounting (external common wiring terminals); (9) represents a mounting substrate; (9A) represents lands for mounting a semiconductor device on the mounting substrate; (10) represents a sealant; (11) represents a flexible board tape; and (12) represents an insulating film (protective film).

[0035]

First of all, flexible wiring board (flexible wiring substrate) (2) is manufactured as shown in Figure 12. As shown in Figure 12, when said flexible wiring board (flexible wiring substrate) (2) is manufactured, wiring is formed on the outer principal surface (first principal surface) of flexible substrate tape (11), with insulating film (protective film) (12) covering it. On the outer principal surface of flexible substrate tape (11) with wiring formed on it as described, wiring (3) for connecting lands (6) for mounting semiconductor chips that have the same function on semiconductor chips (1), lands (4A) for shortcut wiring connection and Au bumps (4) for shortcut wiring connection that connect lands (6) for mounting semiconductor chips and having the same function, of semiconductor chips (1), via (5) for passing said wiring (3) through, and lands (6) for mounting semiconductor chips are formed at their respective positions. On the inner principal surface (second principal surface) of said flexible substrate tape (11), as shown in Figure 13, wiring (3) for connecting lands (6) for mounting semiconductor chips, and having the same function, of semiconductor chips (1), lands (4A) for shortcut wiring connection, as well as Au bumps (4) for shortcut wiring connection and solder ball terminals (7) for mounting are formed.

[0036]

In the method of manufacturing the semiconductor device in Application Example 2, as shown in said Figure 12, flexible wiring board (flexible wiring substrate) (2) is prepared. Then, as shown in Figures 14 and 15, plural semiconductor chips (IC chips) (1) are mounted on lands (6) for carrying semiconductor chips and formed with a prescribed interval on the outer principal surface of said flexible wiring board (2). As shown in Figure 16, semiconductor chips (IC chips) (1) are electrically connected to lands (6) for mounting semiconductor chips by means of external electrodes (Au bumps on the pads) (1A), followed by sealing of the connection region with sealant (sealing resin) (10).

[0037]

As shown in Figure 17, said flexible wiring board (2) having said plural semiconductor chips (1) mounted on it is folded at said double folding portions (2A). As a result, adjacent semiconductor chips (2) mounted on the outer principal surface of said flexible wiring board (2) are superposed back-to-back, and they are fixed together with adhesive (or adhesive tape) (2B). As shown in Figure 17, said flexible wiring board (2) is further folded at said double folding portions (2A), Au bumps (4) for shortcut wiring connection and lands (4A) for shortcut wiring connection are connected, and the next sets of laminates are layered on. In this way, plural sets of laminates are formed.



[0038]

Figures 18(a), (b) show the constitution of said double folded regions. Electrical connection is performed with shortcut wiring portion (2C) of wirings having the same function of the laminates of said plural sets of laminates, so that the wiring length of said flexible wiring board (2) is reduced, and semiconductor device (200) shown in Figure 10 is completed. As shown in Figure 11, for this semiconductor device (200), electrical connection is performed between solder ball terminals (7) for mounting, serving as the external common wiring terminals for wiring having the same function of said laminates, and lands (9A) on assembly substrate (9) for mounting the semiconductor device.

[0039]

As explained above, according to Application Example 2, flexible wiring board (2) that can be folded enables electrical connection among wirings having the same function of the laminates by means of the shortcut wiring portions, and the wiring length of said flexible wiring board (2) is reduced. Consequently, it is possible to prevent signal delay due to the wiring length. Also, in a semiconductor device having a three-dimensional (3D) structure created by folding the wiring board, it is possible to increase the heat dissipation efficiency for the heat generated inside the laminates by means of the shortcut wiring portions for said wirings having the same function of the laminates. Also, it is possible to realize double-sided assembly of IC chips on both surfaces of the board, other than at the solder ball terminal regions for mounting.

[0040]

#### Application Example 3

The semiconductor device in Application Example 3 of the present invention (semiconductor device (300) or (400)) is another application example similar to said Application Example 2, except that shortcut wiring board (8) in Application Example 1 is omitted here. Figures 19 and 20 illustrate the folding structure ((300) and (400)). The manufacturing method is the same as that of said Application Examples 1 and 2.

[0041]

#### Application Example 4

Figure 21 includes a plan view, a lateral cross section and a longitudinal cross section illustrating schematically the constitution of the semiconductor device in Application Example 4 of the present invention. Figure 22 is a lateral cross section illustrating the state in which the semiconductor device of Application Example 4 is mounted on a mounting substrate. As shown

in Figure 21, in the semiconductor device of Application Example 4, plural semiconductor chips (IC memory chips) (1) are mounted at prescribed intervals on the outer principal surface (first principal surface) of flexible wiring board (63) having quarter folding portions (2A). The flexible wiring board is double folded at said double folding portions of said flexible wiring board (63), so that semiconductor chips (1) mounted on the outer principal surface of said flexible wiring board (63) are superposed back-to-back, and are fixed together with adhesive (or adhesive tape). Said flexible wiring board (63) is then quarter folded at said quarter folding portions, and the next sets of laminates are layered on. In this way, plural sets of laminates are formed. Electrical connection is made between lands (61) for shortcut wiring connection of wirings having the same function of the laminates of said plural sets of laminates and solder ball terminals (62) for shortcut wiring, and the wiring length of said flexible wiring board (63) is reduced. Relief hole (26) for relieving the folding stress is formed at the center of said flexible wiring board (63).

[0042]

As shown in Figure 22, semiconductor device (500) of Application Example 4 is mounted on said mounting substrate (9), with electrical connection being made between solder ball terminals (common wiring terminals) (7) for mounting, provided on the inner principal surface (second principal surface) of said flexible wiring board (63), and lands (9A) of mounting substrate (9) for semiconductor device mounting.

[0043]

In the following, an explanation will be given regarding the method of manufacturing the semiconductor device in Application Example 4. Figure 23 is an outer plan view illustrating the wiring constitution of said flexible wiring board (63). Figure 24 is an inner plan view illustrating the wiring constitution of said flexible wiring board (63). Figure 25 is an overall plan view illustrating the state in which semiconductor chips (1) are mounted on said flexible wiring board (63). Figure 26 is a side view of Figure 25. Figure 27 is a cross section illustrating the state in which one semiconductor chip (1) is mounted on the outer principal surface of said flexible wiring board (63). Figure 28 includes a plan view, a lateral cross section, and a longitudinal cross section of double folded flexible wiring board (63) carrying said semiconductor chips (1). Figure 29 is a plan view of the quarter folded flexible wiring board (63) carrying said semiconductor chips (1).

[0044]

In Figures 21-29, (1) represents semiconductor chips (IC chips); (1A) represents the external electrodes of the semiconductor chips (Au bumps on the pads); (3) represents wiring; (6)

represents lands for mounting the semiconductor chips (external common wiring terminals); (7) represents a solder ball terminal for mounting; (9) represents a mounting substrate; (9A) represents lands for mounting semiconductor device on the mounting substrate; (10) represents a sealant; (12) represents an insulating film (protective film); (5) represents via; (17) represents minute (buildup) via; (26) represents a relief hole for relieving the folding stress; (61) represents lands for shortcut connection wiring; (62) represents solder ball terminals for shortcut wiring; and (63) represents a flexible wiring board (flexible wiring substrate) with wiring formed on a polyimide tape.

[0045]

First, flexible wiring board (63) is manufactured as shown in Figure 21. As shown in Figures 23 and 24, when said flexible wiring board (63) is manufactured, wiring is formed on flexible wiring board (63), with an insulating film (protective film) covered on it. On the outer principal surface (first principal surface) of flexible wiring board (63), wiring (3) for connecting lands for mounting semiconductor chips that have the same function on semiconductor chips (1), lands (61) for shortcut wiring connection for connecting the lands for mounting semiconductor chips that have the same function on semiconductor chips (1), bumps of solder ball terminals (62) for shortcut wiring, and lands (6) for mounting semiconductor chips are formed at their respective positions. As shown in Figure 24, wiring (3) for connecting the lands for mounting semiconductor chips that have the same function on semiconductor chips (1), lands 61 for shortcut wiring connection, Au bumps (62) for shortcut wiring connection, and solder ball terminals (7) for mounting are formed on the inner principal surface (second principal surface) of said flexible substrate tape (63).

[0046]

In the method of manufacturing the semiconductor device in Application Example 4, as shown in Figures 23 and 24, flexible wiring board (63) is prepared. Then, as shown in Figures 25 and 26, plural semiconductor chips (IC chips) (1) are mounted on the lands for mounting semiconductor chips and formed at prescribed intervals on the outer principal surface of said flexible wiring board (63). As shown in Figure 27, semiconductor chips (IC chips) (1) are electrically connected to the lands for mounting semiconductor chips by means of external electrodes (Au bumps on the pads) (1A), followed by sealing of the connection region with a sealant (sealing resin).

[0047]

When multi-layer wiring is needed, as shown in Figure 27, a buildup system or the like is adopted for flexible wiring board (63), so that it is possible to form a flexible wiring board (63) having both multi-layer wiring portions that allow high-density wiring (the portion from the left side in the figure to immediately before the thinnest portion to the right of center, and the portion that becomes thicker on the right side) and a foldable portion with single-sided or double-sided mono-layer wiring (the thinnest portion positioned between said multi-layer wiring portions).

[0048]

As shown in Figure 28, said flexible wiring board (63) having said plural semiconductor chips (1) mounted on it is double folded at said double folding portions (2A). As a result, adjacent semiconductor chips (1) mounted on the outer principal surface of said flexible wiring board (63) are superposed back-to-back, and they are fixed together with an adhesive (or adhesive tape). In addition, as shown in Figure 29, said flexible wiring board (63) is quarter folded at said quarter folding portions (2A), and the next sets of laminates are layered. In this way, as shown in Figure 21, plural sets of laminates having semiconductor chips (1) superposed back-to-back are formed. Wirings having the same function of said laminates of said plural sets of laminates are electrically connected by means of short circuit electrodes for creating a shortcut, so that the wiring length of said flexible wiring board (63) is reduced.

[0049]

As shown in Figure 22, semiconductor device (500) of Application Example 4 is assembled on said mounting substrate (9), with electrical connection between external electrodes (7) for mounting, serving as common terminals, provided on the inner principal surface (second principal surface) of said flexible wiring board (63) and lands (9A) of mounting substrate (9) for mounting a semiconductor device. Also, when the folding stress is high, a relief hole (26) for relieving the folding stress can be provided. Also, it is possible to use double-sided mounting of the IC chip on the two surfaces of the board, other than at the solder ball terminal regions for mounting.

[0050]

#### Application Example 5

Figure 30 is a cross section schematically illustrating the state in which the heat absorptive pad of the semiconductor device in Application Example 5 of the present invention is accommodated in the package. Figure 31 is a plan view schematically illustrating the state in which the heat absorptive pad shown in Figure 30 is accommodated in the package. Figure 32 is

a schematic diagram illustrating the constitution of the cooling mechanism with the heat absorptive pad shown in Figure 30.

[0051]

In Figures 30-32, (1) represents semiconductor chips (IC chips); (1A) represents the external electrodes of the semiconductor chips (Au bumps on the pads); (7) represents solder ball terminals for mounting (external common wiring terminals); (26) represents a relief hole for relieving the folding stress; (61) represents lands for shortcut connection wiring; (62) represents solder ball terminals for shortcut wiring; (63) represents a flexible wiring board (flexible wiring substrate) with wiring formed on a polyimide tape; (64) represents a heat absorptive pad; (65) represents a pipe; (66) represents a flow path; (67) represents a fan; (68) represents a heat dissipating part (radiator); (69) represents heat dissipating fins; (70) represents a coolant circulation pump; (71) represents a folded laminated package; and (72) represents a thermoconductive adhesive tape.

[0052]

For the semiconductor device of Application Example 5 of the present invention, laminating is realized by means of cross folding in addition to the bellows folding, double folding and triple [sic; quarter] folding in the aforementioned application examples. As shown in Figures 30 and 31, flexible wiring board (63) (flexible wiring substrate) is quarter folded to laminate semiconductor chips (1). Relief hole (26) for relieving the folding stress is provided at the center of flexible wiring board (63) where the stress is concentrated in cross folding.

[0053]

That is, the semiconductor device has flexible wiring board (63), which has quarter folding portions and relief hole (26) for relieving the folding stress at the center, and which can carry plural semiconductor chips (1) at prescribed intervals on its surface, and plural sets of laminates of semiconductor chips (1) mounted on the outer surface of flexible wiring board (63) and superposed back-to-back when said flexible wiring board (63) is double folded at said double folding portions. Plural semiconductor chips (IC chips) (1) are mounted at the prescribed positions on the outer principal surface of said flexible wiring board (63), and said flexible wiring board (2) is quarter folded at said folding portions (2A), so that semiconductor chips (1) mounted on the outer surface of said flexible wiring board (63) are superposed back-to-back, and are fixed together with adhesive (or adhesive tape) (2B). In addition, said flexible wiring board (63) is quarter folded at said folding portions (2A), and the next set of laminates are layered. In this way, plural sets of laminates are obtained.

[0054]

The thickness of the flexible tape substrate for use in preparing said flexible wiring board (63) may be 75  $\mu\text{m}$ , and the thickness of the Cu wiring may be 35  $\mu\text{m}$ . Wirings having the same function of the laminates of said plural sets of laminates are electrically connected by short circuit electrodes that provide a shortcut, and the wiring length of said flexible wiring board (63) is reduced.

[0055]

As shown in Figures 30 and 31, heat absorptive pad (cooling path) (64) is provided between the laminates with said semiconductor chips superposed. As shown in Figures 30 and 31, said heat absorptive pad (cooling path) (64) is formed with flow path (66). Said heat absorptive pad (cooling path) (64) is fixed by means of thermoconductive adhesive tape (72) between the laminates with said semiconductor chips superposed in a folded stacked laminate package (71).

[0056]

Also, said heat absorptive pad (64) has flow path (66) inside the insulating ceramics or the like used in the IC package. Said flow path (66) goes through pipe (65) and is connected to heat dissipating part (68), and it is filled with water or other liquid. Attachment of heat absorptive pad (64) is performed by means of thermoconductive adhesive tape (72). Also, silicon grease together with an adhesive material can be used for even better performance. Coolant circulating pump (70) force-circulates the internal liquid, and the heat absorbed with heat absorptive pad (64) is transported, with the circulating liquid serving as a medium, through pipe (65) to heat dissipating part (68), and is subjected to forced cooling by fan (67). The liquid cooled in heat dissipating part (68) passes through pipe (65) back to heat absorptive pad (64). Also, a heat pipe, heat dissipating plate, or the like can be incorporated, or a heat sink attached.

[0057]

When multi-layer wiring is needed, as shown in Figure 27, a buildup system or the like is adopted for flexible wiring board (63), so that it is possible to form a flexible wiring board (63) having both multi-layer wiring portions that allow high-density wiring (the portion from the left side in the figure to immediately before the thinnest portion to the right of the center, and the portion that becomes thicker on the right side) and the foldable portion with the single-sided or double-sided mono-layer wiring (the thinnest portion positioned between said multi-layer wiring portions).

[0058]

Said buildup multi-layer wiring portion can be prepared as follows: Wiring (3) is formed with copper or another electroconductive substance on polyimide tape (flexible substrate) (63), followed by laminating insulating photosensitive resin (18). Then, by means of exposure, fine (buildup) via (17) is opened, while the remaining portion is cured to form an insulating layer, and wiring (3) is formed of copper or other electroconductive substance. Consequently, it can be manufactured using the same method as minute (buildup) via (17) even for the foldable portion of a mono-layer wiring.

[0059]

In Application Examples 1-5, the manufacturing method makes use of bare chip assembly by means of Au bumps. However, other manufacturing methods may also be adopted, such as wiring bonding, beam leads, etc. Also, in said application examples, the semiconductor device and its manufacturing method have been explained. However, as can be seen from the aforementioned explanation, the present invention is also applicable to a semiconductor module and its manufacturing method.

[0060]

In the above, the present invention has been explained with reference to application examples. However, the present invention is not limited to the aforementioned application examples. Various modifications are allowed as long as the gist of the present invention is observed.

[0061]

#### Effect of the invention

The following is a brief account of the effect of the invention disclosed in the present patent application. According to the present invention, in a semiconductor device or semiconductor module with a three-dimensional (3D) structure created by folding a flexible wiring board, short circuit electrodes that provide wiring shortcuts are used for electrical connection so as to reduce the wiring length. Consequently, it is possible to prevent signal delay due to the wiring length. Also, by providing a heat absorptive pad (cooling path) between the laminates when said semiconductor chips are superposed, it is possible to increase the heat dissipation efficiency.

### Brief description of the figures

Figure 1 is a front view schematically illustrating the constitution of the semiconductor device in Application Example 1 of the present invention.

Figure 2 is a front view of the semiconductor device of Application Example 1 assembled on a mounting substrate.

Figure 3 is an outer plan view illustrating the wiring constitution of the flexible wiring board in Application Example 1.

Figure 4 is an inner plan view illustrating the wiring constitution of the flexible wiring board of Application Example 1.

Figure 5 is an overall plan view illustrating the state in which the semiconductor chips are mounted on the flexible wiring board of Application Example 1.

Figure 6 is a side view of Figure 5.

Figure 7 is a cross section illustrating the state in which a semiconductor chip is mounted on the flexible wiring board in Application Example 1.

Figure 8 is a plan view illustrating the constitution of the wiring board serving as one and the other shortcut wiring boards in Application Example 1.

Figure 9 is a diagram illustrating the state in which one of the shortcut wiring boards is connected to the wiring of the flexible wiring board in Application Example 1.

Figure 10 is a front view schematically illustrating the semiconductor device in Application Example 2 of the present invention.

Figure 11 is a front view of the semiconductor device mounted on the mounting substrate in Application Example 2.

Figure 12 is an outer plan view illustrating the wiring constitution of flexible wiring board (2) in Application Example 2.

Figure 13 is an inner plan view illustrating the wiring constitution of the flexible wiring board in Application Example 2.

Figure 14 is an overall plan view illustrating the state in which the semiconductor chips are mounted on the flexible wiring board in Application Example 2.

Figure 15 is a side view of Figure 14.

Figure 16 is a cross section illustrating the state in which a semiconductor chip is mounted on the flexible wiring board in Application Example 2.

Figure 17 is a diagram illustrating the state in which the flexible wiring board having semiconductor chips mounted on it is folded in Application Example 2.

Figure 18 is an enlarged cross section illustrating the state in which the flexible wiring board is folded at the double folding portions of the flexible wiring board in Application Example 2.



Figure 19 includes a front view, plan view, and side view illustrating schematically the constitution of the semiconductor device in Application Example 3 of the present invention.

Figure 20 is a front view schematically illustrating the constitution of the semiconductor device in Application Example 3.

Figure 21 includes a plan view, a lateral cross section and a longitudinal cross section illustrating schematically the constitution of the semiconductor device in Application Example 4 of the present invention.

Figure 22 is a lateral cross section of mounting of the semiconductor device on the mounting substrate in Application Example 4.

Figure 23 is an outer plan view illustrating the wiring constitution of the flexible wiring board in Application Example 4.

Figure 24 is an inner plan view illustrating the wiring constitution of the flexible wiring board in Application Example 4.

Figure 25 is an overall plan view illustrating the state in which semiconductor chips are mounted on the flexible wiring board in Application Example 4.

Figure 26 is a side view of Figure 25.

Figure 27 is a cross section illustrating the state in which a semiconductor chip is mounted on said flexible wiring board (when a multi-layer wiring is adopted) in Application Example 4.

Figure 28 includes a plan view, a lateral cross section and a longitudinal cross section of the double folded flexible wiring board having semiconductor chips mounted on it in Application Example 4.

Figure 29 is a plan view of the quarter folded flexible wiring board having semiconductor chips mounted on it in Application Example 4.

Figure 30 is a cross section schematically illustrating the state in which the heat absorptive pad of the semiconductor device is accommodated in the package in Application Example 5 of the present invention.

Figure 31 is a plan view schematically illustrating the state in which the heat absorptive pad is accommodated in the package in Application Example 5.

Figure 32 is a schematic diagram schematically illustrating the constitution of the cooling mechanism using the heat absorptive pad in Application Example 5.

#### Explanation of reference symbols

- 1 Semiconductor chip (IC chip)
- 1A External electrodes of semiconductor chip
- 2 Flexible wiring board

- 2A Folding portion
- 2B Adhesive for semiconductor chip
- 2C Shortcut wiring connecting portion
- 3 Wiring
- 4 Au bump for shortcut wiring connection
- 4A Land for shortcut wiring connection
- 5 Via
- 6 Land for mounting semiconductor chip
- 7 Solder ball terminal for mounting
- 8A, 8B Shortcut wiring board
- 9 Mounting substrate
- 9A Land for mounting of semiconductor device
- 10 Sealant
- 11 Flexible substrate tape
- 12 Insulating film (protective film)
- 17 Minute (buildup) via
- 18 Insulating photosensitive resin
- 22 Adhesive tape
- 23 Solder
- 26 Relief hole for relieving the folding stress
- 61 Land for shortcut wiring connection
- 62 Solder ball terminal for shortcut wiring
- 63 Flexible wiring board
- 64 Heat absorptive pad
- 65 Pipe
- 66 Flow path
- 67 Fan
- 68 Heat dissipating part (radiator)
- 69 Heat dissipating fins
- 70 Coolant circulating pump
- 71 Folding laminated package
- 72 Thermoconductive adhesive tape

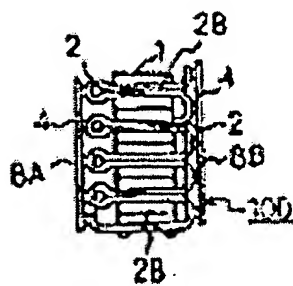


Figure 1

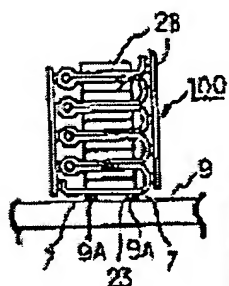


Figure 2

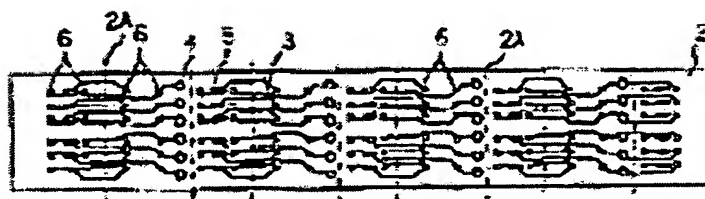


Figure 3

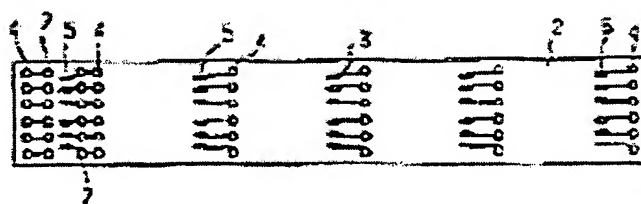


Figure 4

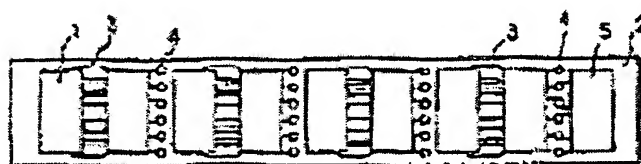


Figure 5



Figure 6

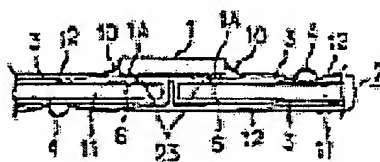


Figure 7

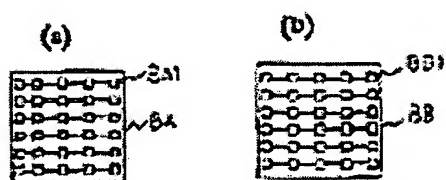


Figure 8

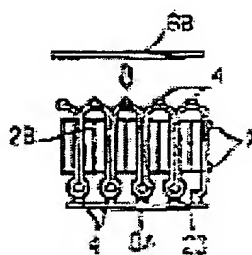


Figure 9

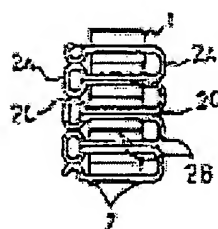


Figure 10

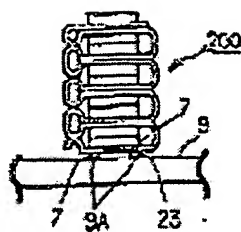


Figure 11

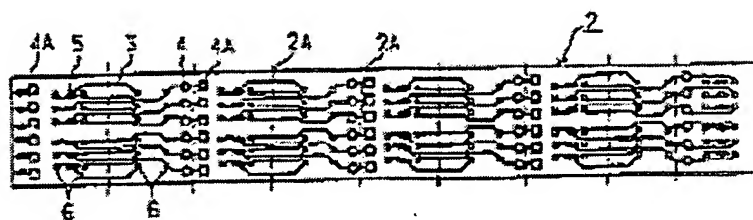


Figure 12

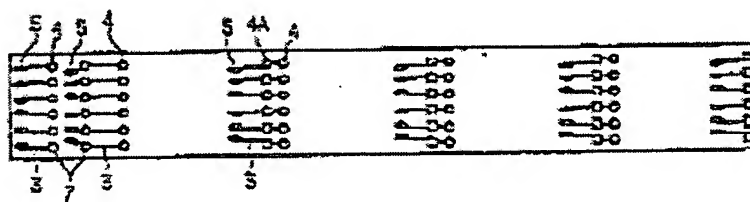


Figure 13

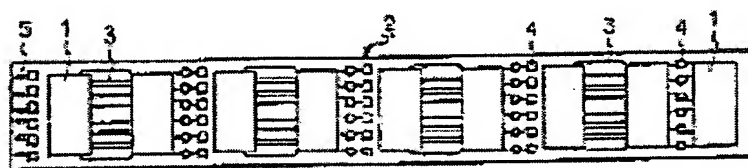


Figure 14

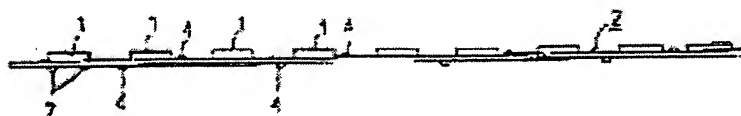


Figure 15

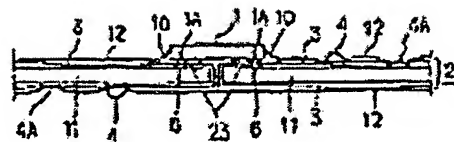


Figure 16

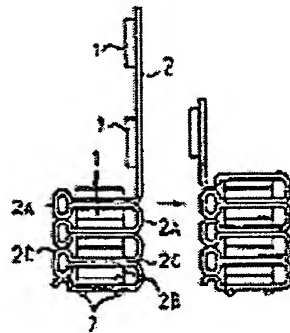


Figure 17

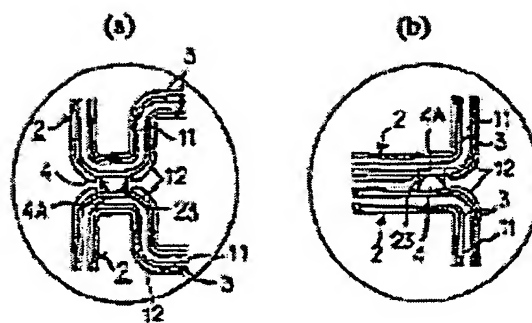


Figure 18

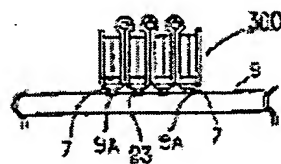


Figure 19

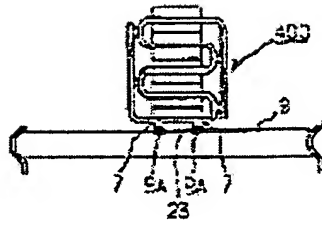


Figure 20

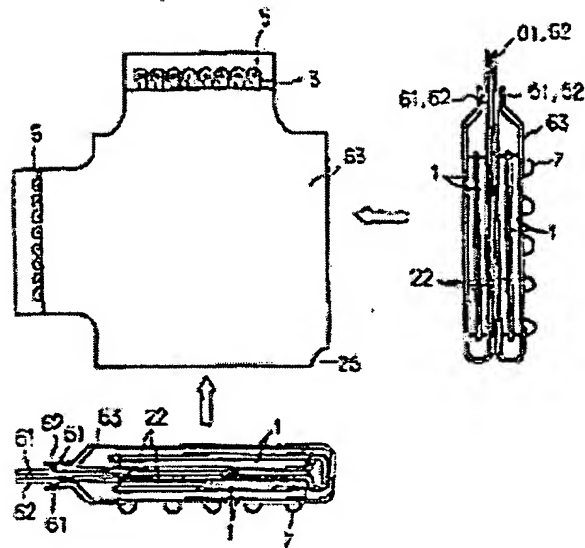


Figure 21

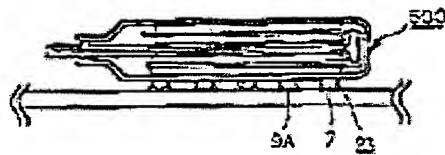


Figure 22

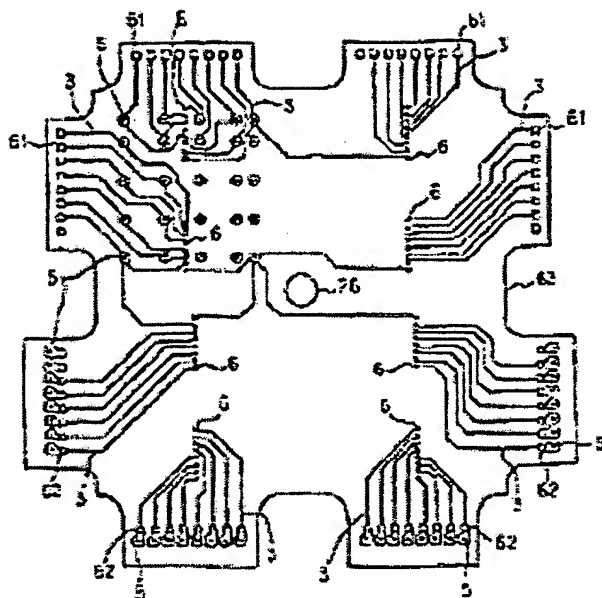


Figure 23

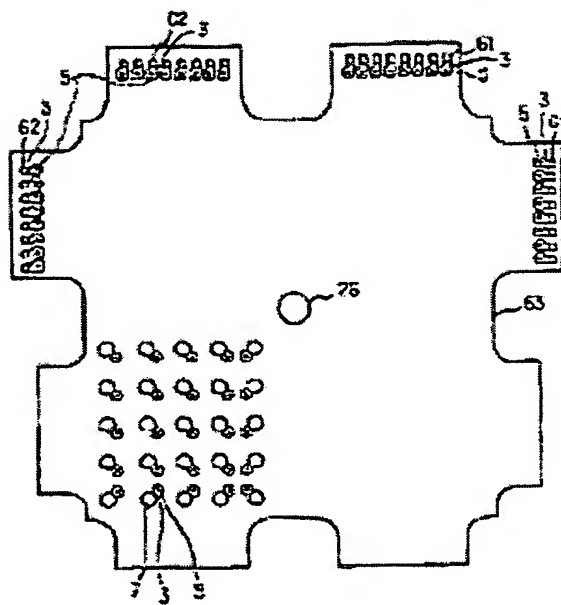


Figure 24



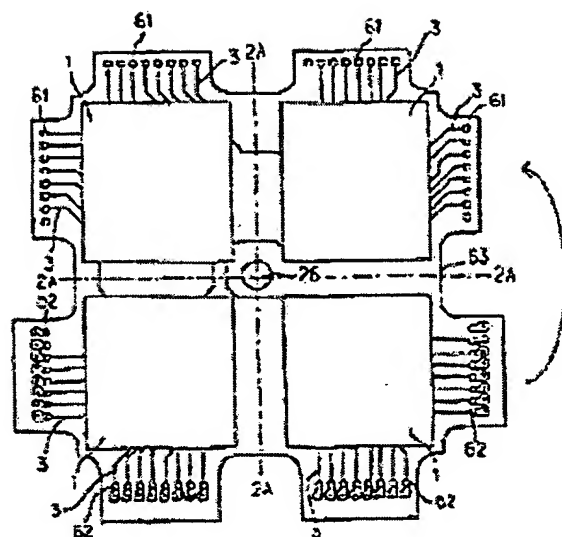


Figure 25

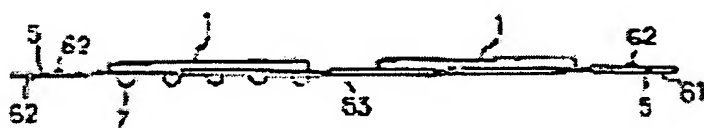


Figure 26

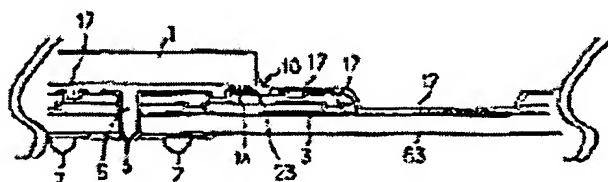


Figure 27





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